1.1.1 The Institution ensures effective curriculum planning and delivery through a well-planned and documented process including Academic calendar and conduct of continuous internal Assessment

❖ **Additional information/ Supporting Documents**

1. Academic Calendar of Institute
2. Academic Calendar of affiliating University
3. Teaching Schemes of all branches
4. Internal & External evaluation directions
5. Unit Test Time Table
6. Unit Test Question Paper Format
7. Teaching Plan
8. Syllabus Completion Report
9. Remedial Classes Notice
10. Laboratory Manual
11. Photos Showing use of ICT
12. Academic Audit Report submitted by Institutional IQAC to CDC

1. Academic Calendar of Institute

Paramhansa Ramkrishna Maunibaba Shikshan Sanstha's

Anuradha Engineering College, Chikhli

Anuradha Nagar, Sakegaon Road, Chikhli Dist. Buldhana M.S. 443 201

Approved by AICTE New Delhi and State Government of Maharashtra

Permanently Affiliated by Sant Gadge Baba Amravati University, Amravati.

www.aecc.ac.in

Date: 15/07/2022

Academic Calendar 2022-23

Sr. No.	Activity	Date / Duration
	Teaching Days (Odd Semester)	**25th July 2022 – 22nd Oct. 2022 (71)** **9th Nov. 2022 – 30th Nov. 2022 (19)**
01	**College opening for ODD Semester**	**25th July 2022**
02	Registration	25th July 2022
03	Mohram (Holiday)	09th August 2022
04	Rakshabhandahan (Holiday)	11th August 2022
05	Independence day celebration (Holiday)	15th August 2022
06	Parshi New Year (Pateti) (Holiday)	16th August 2022
07	Ganesh Chaturthi (Holiday)	31th August 2022
08	Ganesh Festival 2022	31th August -2nd Sept. 2022
09	Teachers day celebration (5th September)	6th September 2022
10	Anant Chaturdashi (Holiday)	9th September 2022
11	Blood Donation/Eye Camp	12th September 2022
12	Engineer's Day Celebration / Final Year Seminar Presentation	15th September 2022 15th September – 22nd September 2022
13	**First** Unit Test (Odd Semester)	28,29,30 September 2022
14	Dasara (Holiday)	5th October 2022
15	Declaration of result (First Unit Test)	7th October 2022
16	Diwali Vacation	24th October - 8th November 2022
17	**Second** Unit Test (Odd Semester)	17,18,19 November 2022
18	Declaration of result (Second Unit Test)	25th November 2022
19	**Last Day of Odd Semester**	**30th November 2022**
20	**Winter Vacation** (Diwali Vacation)	**24th October - 8th November 2022**
21	Odd Semester University Examinations	1st December 2022 – 21 January 2023
22	**College opening for Even semester**	**23rd January 2023**
23	Republic Day (Holiday)	26th January 2023
24	Sport Festival - **Ashwamedh – 2023,** Annual Social Gathering **Anuspark-2023,** **Alumni Meet – 2023, N.S.S.** Camp	**23rd January – 31th January 2023**
25	**Teaching days (Even Semester)**	**1st February – 27th May 2023 (91)**
26	Mahashivratari (Holiday)	18th February 2023
27	Holi (Dhulivandan)(Holiday)	7th March 2023
28	Gudhi Padva (Holiday)	22nd March 2023
29	**First** Unit Test (Even Semester)	27th -29th March 2023
30	Shriram Navmi (Holiday)	30th March 2023
31	Mahavir Jayanti (Holiday)	4th April 2023
32	Declaration of result (first unit test)	6th April 2023
33	Good Friday (Holiday)	7th April 2023
34	Dr.Babasaheb Ambedkar Jayanti (Holiday)	14th April 2023
35	Ramzan Id (Holiday)	22nd April 2023

Paramhansa Ramkrishna Maunibaba Shikshan Sanstha's
Anuradha Engineering College, Chikhli
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Sr. No.	Activity	Date / Duration
36	AnuradhaTai Memorial Day /Maharashtra Day	1st May 2023
37	Buddha Pournima (Holiday)	5th May 2023
38	International Conference (ICGTSD2023)/ Campus Recruitment /Training Program	8th -9th May 2023
39	**Second** Unit Test (Even Semester)	18th -20th May 2023
40	Final Year Project Exhibition 2023	24th May 2023
41	Declaration of result (Second Unit Test)	25th May 2023
42	**Last Day of Even Semester**	**27th May 2023**
43	Even Semester University Examinations	29th May 2023 – 1st July 2023
44	**Second Term Vacation**	**29th May 2023 – 1st July 2023**
45	Commencement of Next Academic Session 2023-24	3rd July 2023

15/7/2023

Dr. A. S. Kapse
Dean Academics

ANURADHA ENGINEERING COLLEGE F740-89-203(E)/RC/94 CHIKHLI - 443201

Dr. Arun Nanhai
Principal
PRINCIPAL
Anuradha Engineering College
CHIKHLI Dist. Buldana

Copy To:

1. Dean R & D
2. H.O.D., Mech. Deptt.
3. Librarian
4. First Year Co-ordinator
5. H.O.D., CSE Deptt.
6. H.O.D., IT Deptt.
7. H.O.D., Chemical Deptt.
8. H.O.D., E&TC. Deptt.
9. H.O.D., Text. Deptt.
10. H.O.D., Sport Deptt.
11. Office
12. Store In charge
13. Security In charge

2. Academic Calendar of affiliating University

SANT GADGE BABA AMRAVATI UNIVERSITY GAZETTE

Official Publication of Sant Gadge Baba Amravati University

PART TWO

(असाधारण)

सोमवार, दिनांक २७ जून, २०२२

अधिसूचना

क्रमांक : ७४/२०२२ **दिनांक**: २७/६/२०२२

विषय : **शैक्षणिक नियामिका .... शैक्षणिक वर्ष २०२२-२०२३**
Subject : **Academic Calendar.... Academic Year 2022-2023**

सर्व संबंधितांच्या माहिती करीता अधिसूचित करण्यात येते की, शैक्षणिक वर्ष २०२२-२०२३ ची शैक्षणिक नियामिका खालील प्रमाणे राहील.

It is notified for all concerned that, the Academic Calendar for the Academic Session 2022-2023 shall be as under:

तक्ता -१
(Table-1)

अ. क्र. (S. N)	कृती/कार्यक्रम (Activity)	प्रारंभ (Commencement)	समाप्ती (Cessation)	एकूण दिवस (Total Days)
१.	शैक्षणिक सत्र (प्रथम सत्र) Academic Session (First Session)	शुक्रवार, दि. १ जुलै, २०२२ Friday, 1st July, 2022	बुधवार, दि. ३० नोव्हेंबर, २०२२ Wednesday, 30th November, 2022	110
२.	प्रवेश प्रक्रीया % Admission Process	शुक्रवार, दि. १ जुलै, २०२२ Friday, 1st July, 2022	शनिवार, दि. १६ जुलै, २०२२ Saturday, 16th July, 2022	14
३.	अभिक्रम प्रक्रिया (प्रथम वर्ष प्रवेशित विद्यार्थ्याकरिता) Induction Programme (For 1st Year Students)	सोमवार, दि. १८ जुलै, २०२२ Monday, 18th July, 2022	शनिवार, दि. २३ जुलै, २०२२ Saturday, 23rd July, 2022	06
४.	शैक्षणिक दिवस (विषम सत्र) Teaching Days (Odd Semesters)	सोमवार, दि. २५ जुलै, २०२२ Monday, 25th July, 2022	शनिवार, दि. २२ ऑक्टोबर, २०२२ Saturday, 22nd October, 2022	71
		बुधवार, दि. ९ नोव्हेंबर, २०२२ Wednesday, 9th November, 2022	बुधवार, दि. ३० नोव्हेंबर, २०२२ Wednesday, 30th November, 2022	19
				90
५.	प्रथम सत्र अवकाश (First Term Vacation)	सोमवार, दि. २४ ऑक्टोबर, २०२२ Monday, 24th October, 2022	मंगळवार, दि. ८ नोव्हेंबर, २०२२ Tuesday, 8th November, 2022	16

६.	विषम सत्रांची विद्यापीठीय परीक्षा/ अशैक्षणिक दिवस Odd Semesters University Examinations/ Non-instructional days	गुरूवार, दि. १ डिसेंबर, २०२२ Thursday,1st December, 2022	शनिवार, दि. २१ जानेवारी, २०२३ Saturday, 21st January, 2023	45
७.	शैक्षणिक सत्र (द्वितीय सत्र) Academic Session (Second Session)	सोमवार, दि. २३ जानेवारी, २०२३ Monday, 23rd January, 2023	शनिवार, दि. २७ मे, २०२३ Saturday, 27th May, 2023	98
८.	अशैक्षणिक दिवस Non-instructional days (For N.S.S., Gathering etc.)	सोमवार, दि. २३ जानेवारी, २०२३ Monday, 23rd January, 2023	मंगळवार, दि. ३१ जानेवारी, २०२३ Tuesday, 31st January, 2023	7
९.	शैक्षणिक दिवस (सम सत्र) Teaching Days (Even Semesters)	बुधवार, दि. १ फेब्रुवारी, २०२३ Wednesday, 1st February, 2023	शनिवार, दि. २७ मे, २०२३ Saturday, 27th May, 2023	91
१०.	सम सत्रांची विद्यापीठीय परीक्षा Even Semesters University Examination	सोमवार, दि. २९ मे, २०२३ Monday, 29th May, 2023	शनिवार, दि. १ जुलै, २०२३ Saturday, 1st July, 2023	29
११.	द्वितीय सत्र अवकाश (Second Term Vacation)	सोमवार, दि. २९ मे, २०२३ Monday, 29th May, 2023	शनिवार, दि. १ जुलै, २०२३ Saturday, 1st July, 2023	34
१२.	पुढील शैक्षणिक सत्राचा २०२३-२०२४ चा प्रारंभ Commencement of Next Academic Session 2023-2024	सोमवार, दि. ३ जुलै, २०२३ Monday, 3rd July, 2023		

% सर्व विद्याशाखांच्या पदवी आणि पदव्युत्तर अभ्यासक्रमांसाठी विद्यापीठ अनुदान आयोग/ए.आय.सी.टी.ई./शिखर संस्था, महाराष्ट्र शासन आणि विद्यापीठाने वेळोवेळी निर्गमित केलेल्या निर्देशानुसार प्रवेश प्रक्रिया राबविण्यात यावी.
(% Admission Procedure should be continued as per the directions issued by UGC/AICTE/Appenx Bodies, Government of Maharashtra and University from time to time for all degrees and post graduate programmes of all faculties.)

कोवीड-१९ संबंधित विहित मार्गदर्शक तत्त्वांचे अनुसरण करुन वर्गकक्ष ऑनलाईन / ऑफलाईन (वर्गकक्ष) किंवा मिश्रित स्वरुपात (ऑनलाईन + ऑफलाईन) सुरु केले जाऊ शकतात.
(The classes may be started in online/ offline (class room) or blended mode (online+offline) following the prescribed protocols /guidelines related to COVID-19.)

विशेष सुचना: (Special Note):

विद्यापीठाचा दीक्षांत समारंभ मंगळवार, दि. २० डिसेंबर, २०२२ रोजी आयोजित करण्यात येईल.
University Convocation will be organized on Tuesday, 20th December, 2022.

1. ही शैक्षणिक नियामिका विद्यापीठाचे शैक्षणिक विभाग/ घटक महाविद्यालये/ संलग्नित महाविद्यालये (व्यावसायिक महाविद्यालयांसहीत) यांना लागू राहील.
(This Academic Calendar shall be applicable to all University Teaching Departments/ University Constituent Colleges/Affiliated Colleges (including Professional Colleges) of Sant Gadge Baba Amravati University.)

2. विद्यापीठाच्या शैक्षणिक विभागांतील / घटक महाविद्यालयातील/ संलग्नित महाविद्यालयांतील शिक्षक व शैक्षणिक कर्मचा-यांना तक्ता-२ मध्ये दर्शविण्यात आलेल्या सुट्यांव्यतिरिक्त राज्य शासनाने जाहीर केलेल्या इतर सुट्या अथवा जिल्हाधिका-यांनी जाहीर केलेल्या सुट्या उपभोगता येणार नाहीत. तथापि, यासंदर्भात अनुषंगिक निर्णय घेण्याचे अधिकार मा. कुलगुरु यांना राहतील.

(The Teaching Departments of the University/ University Constituent Colleges/ Affiliated Colleges of the University shall have holidays as per Table-2 and shall not avail the holidays declared by the State Government or the District Collector. However, the Hon'ble Vice-Chancellor shall have the power to take decision in this regard.)

3. परीक्षा कालावधी कमी करण्यात यावा, ज्यामुळे मूल्यांकनाला पुरेसा वेळ देता येईल व निकाल वेळेवर जाहीर करता येतील, तथा प्रवेश प्रक्रियेला गती देवून प्रवेश वेळेत पूर्ण करता येतील. जेणेकरुन विद्यार्थी महाविद्यालय/ विद्यापीठ परिसरात शैक्षणिक कार्यासाठी नियोजित कार्यक्रमानुसार उपस्थित राहू शकेल. याकरीता परीक्षा विभागाने परीक्षेकरिता निर्धारीत केलेल्या कालावधीचे कटाक्षाने पालन करावे.

(Span of Examination be curtailed to have enough time for evaluation and the publication of results in time so that the admission process could be speed up and completed in time, to have students' presence in the campus for teaching as per schedule. For this, the time span allotted for examinations shall be strictly followed by Examination Section.)

4. अभिक्रम प्रक्रिया : शिखर संस्थांच्या (ए.आय.सी.टी.ई., यु.जी.सी. इत्यादी) मार्गदर्शक तत्त्वांनुसार विद्यापीठाच्या शैक्षणिक विभागाद्वारे/ घटक महाविद्यालयाद्वारे/ संलग्नित महाविद्यालयांद्वारे अभिक्रम प्रक्रिया अंतर्गत विविध उपक्रम राबविण्यात यावेत.

Induction Programme: Activities shall be performed as per guidelines of the apex bodies (A.I.C.T.E., U.G.C. etc.) by the University teaching departments/ constituent / affiliated colleges.

तक्ता -२

(Table – 2)

अ. क्र. (Sr.No.)	सण/सुट्या (Festivals/Holidays)	दिवस व दिनांक (Day & Date)
१.	मोहरम Moharum	मंगळवार, दि. ९ ऑगस्ट, २०२२ Tuesday, 9th August, 2022
२.	रक्षाबंधन Rakshabandhan	गुरूवार, दि. ११ ऑगस्ट, २०२२ Thursday, 11th August, 2022
३.	स्वातंत्र्य दिन Independence Day	सोमवार, दि. १५ ऑगस्ट, २०२२ Monday, 15th August, 2022
४.	पारशी नूतनवर्ष (शहेनशाही) Parsi New Year (Shahenshahi)	मंगळवार, दि. १६ ऑगस्ट, २०२२ Tuesday, 16th August, 2022
५.	श्रीगणेश चतुर्थी ShriGanesh Chaturthi	बुधवार, दि. ३१ ऑगस्ट, २०२२ Wednesday, 31st August, 2022
६.	अनंत चतुर्दशी Anant Chaturdashi	शुक्रवार, दि. ९ सप्टेंबर, २०२२ Friday, 9th September, 2022
७.	दसरा Dasara	बुधवार, दि. ५ ऑक्टोबर, २०२२ Wednesday, 5th October, 2022

८.	प्रजासत्ताक दिन Republic Day	गुरूवार, दि. २६ जानेवारी, २०२३ Thursday, 26th January, 2023
९.	महाशिवरात्री Mahashivratri	शनिवार, दि. १८ फेब्रुवारी, २०२३ Saturday, 18th February, 2023
१०.	होळी (दुसरा दिवस) Holi (Second Day)	मंगळवार, दि. ७ मार्च, २०२३ Tuesday, 7th March, 2023
११.	गुढीपाडवा Gudhi Padwa	बुधवार, दि. २२ मार्च, २०२३ Wednesday, 22nd March, 2023
१२.	श्रीराम नवमी Shriram Navmi	गुरूवार, दि. ३० मार्च, २०२३ Thursday, 30th March, 2023
१३.	महावीर जयंती Mahavir Jayanti	मंगळवार, दि. ४ एप्रिल, २०२३ Tuesday, 4th April, 2023
१४.	गुड फ्रायडे Good Friday	शुक्रवार, दि. ७ एप्रिल, २०२३ Friday, 7th April, 2023
१५.	डॉ.बाबासाहेब आंबेडकर जयंती Dr.Babasaheb Ambedkar Jayanti	शुक्रवार, दि. १४ एप्रिल, २०२३ Friday, 14th April, 2023
१६.	रमझान ईद (ईद-उल-फितर) Ramzan Id (Id-Ul-Fitar)	शनिवार, दि. २२ एप्रिल, २०२३ Saturday, 22nd April, 2023
१७.	महाराष्ट्र दिन Maharashtra Day	सोमवार, दि. १ मे, २०२३ Monday, 1st May, 2023
१८.	बुध्द पौर्णिमा Buddha Pournima	शुक्रवार, दि. ५ मे, २०२३ Friday, 5th May, 2023

स्वा/-
(डॉ.टी.आर.देशमुख)
कुलसचिव,
संत गाडगे बाबा अमरावती विद्यापीठ

*****

1.1.1 **The Institution ensures effective curriculum planning and delivery through a well-planned and documented process including Academic calendar and conduct of continuous internal Assessment**

3. Teaching Schemes of all branches

(10) Subject to his/her compliance with the provisions of this Direction & other Ordinances pertaining to Examination in force from time to time, the applicant for admission, at the end of the course of study of a particular semester/session, to an Examination specified in column (1) of the table I below, shall be eligible to appear if,

i) he/she satisfies with the conditions in the table and the provisions there under.
ii) he/she complies with the provisions of the ordinance pertaining to the Examination in general from time to time.
iii) he/she has prosecuted a regular course of study in a college affiliated to the University.

iv) he/she has in the opinion of the Principal shown satisfactory progress in his/her studies.

TABLE I

Name of Exam B.E./B.Text.E./ B.Tech. (Chem. Engg.)/B.Tech. (Chem.Tech.) Polymer (Plastic)Tech.	The student should have passed Exam. of	The Student should have satisfactorily completed the following semester	The student should have passed the following examination
1.	2.	3.	
First Semester Group A/Group B	XII standard Examination or equivalent	....	....
Second Semester Group A/Group B	....	I Semester Group A/Group B	.....
Third Semester	....	II Semester Group A/Group B	2/3rd heads of I & II Sem. combined together
Fourth Semester	.....	III Semester	.....
Fifth Semester	I & II Sem.	IV Semester	2/3rd heads of III & IV Sem. combined together
Sixth Semester	....	V Semester	.....
Seventh Semester	III & IV Sem. combined together	VI Semester	2/3rd heads of V & VI Sem.
Eighth Semester	.....	VII Semester	.....

(11) An examinee who has passed 2/3 rd heads of passing shall be allowed to keep term in the next higher class.
Explanation:
(i) While calculating 2/3 rd heads of passing, fraction if any shall be ignored
(ii) For considering the heads of passing, every theory and every practical shall be considered as separate head of passing.

(12) The schemes of teaching & examinations shall be as provided under "**Appendix-A**" appended with this Direction.

(13) The fees for each B.E./B.Text.E./B.Tech. (Chem. Engg.)/B.Tech. (Chem. Tech.) Polymer (Plastic) Tech. Examinations (Theory & Practical) shall be as prescribed by University from time to time.

(14) The computation of Semester Grade Point Average (SGPA) and Cumulative Grade Point Average (CGPA) of an examinee shall be done as given below :-

The marks will be given in all examinations which will include college assessment marks and the total marks for each Theory / Practical shall be converted into Grades as per **Table II**.

SGPA shall be calculated based on Grade Points corresponding to Grade as given in Table II and the Credits allotted to respective Theory / Practical shown in the scheme for respective semester.

SGPA shall be computed for every semester and CGPA shall be computed only in VIII semester. The CGPA of VIII semester shall be calculated based on SGPA of VII and SGPA of VIII semester as per following computation :-

$$SGPA = \frac{C_1 \times G_1 + C_2 \times G_2 + ... + C_n G_n}{C_1 + C_2 + ... + C_n}$$

Where, C_1 = Credit of individual Theory / Practical
G_1 = Corresponding Grade Point obtained in the respective Theory / Practical

$$CGPA = \frac{(SGPA)_{VII} \times (Cr)_{VII} + (SGPA)_{VIII} \times (Cr)_{VIII}}{(Cr)_{VII} + (Cr)_{VIII}}$$

Where, $(SGPA)_{VII}$ = SGPA of VII Semester
$(Cr)_{VII}$ = Total Credits for VII Semester
$(SGPA)_{VIII}$ = SGPA of VIII Semester
$(Cr)_{VIII}$ = Total Credits for VIII Semester

CGPA equal to 6.00 and above shall be considered as equivalent to First Class which shall be mentioned on Grade Card of VIII Semester as a foot note.

TABLE II
THEORY

Grade	Percentage of Marks	Grade Points
AA	80 ≤ Marks ≤ 100	10
AB	70 ≤ Marks < 80	9
BB	60 ≤ Marks < 70	8
BC	55 ≤ Marks < 60	7
CC	50 ≤ Marks < 55	6
CD	45 ≤ Marks < 50	5
DD	40 ≤ Marks < 45	4
FF	00 ≤ Marks < 40	0
ZZ	Absent in Examination	—

PRACTICAL

Grade	Percentage of Marks	Grade Points
AA	85 ≤ Marks ≤ 100	10
AB	80 ≤ Marks < 85	9
BB	75 ≤ Marks < 80	8
BC	70 ≤ Marks < 75	7
CC	65 ≤ Marks < 70	6
CD	60 ≤ Marks < 65	5
DD	50 ≤ Marks < 60	4
FF	00 ≤ Marks < 50	0
ZZ	Absent in Examination	—

(15) (i) The scope of the subjects shall be as indicated in the syllabi.
(ii) The medium of instruction and examination shall be English.

(16) The Schemes of teaching & examination of Semester I & II (Group A & B) of B.E. /B.Text. E./B.Tech. (Chem.Engg.)/ B.Tech. (Chem. Tech.) (Polymer) (Plastic) Tech. had been already implemented from the session 2019-2020 which was notified vide Direction No. 26/2019.

(17) As per A.I.C.T.E. Model Curriculum, an Induction Program of three (3) weeks duration is mandatory to the students at the start of the first semester.

(18) The Schemes of teaching & examination of Semester III to VIII of B.E./ B.Text.E./ B.Tech. (Chem.Engg.) (C.B.C.S.) of the branches Civil Engg., Mechanical Engg., Electronics & Telecommunication Engg., Computer Science & Engg., Computer Engg., Electrical Engg., Electrical Engg. (Electronics & Power), Electrical & Electronics Engg., Information Technology, Textile Engg., Chemical Engg., (C.B.C.S.) as per A.I.C.T.E. Model Curriculum shall be implemented in phase wise manner as under :

(i) For Semester III & IV from the session - 2020-2021
(ii) For Semester V & VI from the session - 2021-2022
(iii) For Semester VII & VIII from the session - 2022-2023

(19) The Schemes of teaching & examination of Semester I & II of B.E. / B.Text.E./ B.Tech. (Chemical Engg.) (common to all branches) and Semester III to VIII of the branches Civil Engg., Mechanical Engg., Electronics & Telecommunication Engg., Computer Science & Engg., Computer Engg., Electrical Engg., Electrical Engg. (Electronics & Power), Electrical & Electronics Engg., Information Technology, Textile Engg., Chemical Engg., (C.B.C.S.) as per A.I.C.T.E. Model Curriculum shall be as per Appendices A,B,C,D,E,F,G,H,I,J,K and L appended with this Direction.

(20) (i) The Semester wise chart regarding the workload and Credits as per A.I.C.T.E. Model Curriculum guidelines for Engineering & Technology Courses for the Schemes of teaching & examination of Sem. III to VIII is as under :

CHART

Sem.	Theory	Pract.	Theory credits	Pract. Credits	Semester Credits	Hours/ week	Remarks
I	4	4	15	5	20	25	Started from session 2019-20
II	4	4	15	5	20	25	
III	5	4	16	4	20	26	ES 2T, 0 credit
IV	5	4	18	4	22	26	ES 2T, 2 credits
V	5	4	16	4	20	24	PE-1,OE-1
VI	5	4	16	4	20	24	PE-1,OE-1
VII	5	3	16	3+4	23	30	PE-2 or 3, Project seminar - 8 hrs, 4 credits
VIII	4	2	12	2+6	20	28	PE-1 or 2, Project seminar 12hrs, 6 credits
Total	**37**	**29**	**124**	**41**	**165**		

(ii) The workload for the subject Environment Studies for Semester III & IV (3ES06 & 4ES06) which is common for all branches in all the Faculties as per Ordinance No. 42/2005 is as : 2 theory in III semester with no credits, 2 theory in IV semester with 2 credits and examination at the end of IV semester at college level having distribution as : 80 (Max. marks for Theory) + 20 (Internal) = 100 (Total marks) – 40 (Minimum marks for passing)

(iii) Open Electives (OE): Open Elective to be opted from the courses offered by other disciplines of Engineering & Technology of the university / Massive Open learning Courses (MOOC) such as SWAYAM pertaining to the profession.

(iv) Students completing foreign language course or completing minimum 4 weeks internship (Full time in Vacations) or participating in sports at National / International level shall be exempted from O.E. in the same / adjacent semester.

(v) An Orientation Program of 15 hours duration /MOOC to be offered to the students during (a)VthSemester : Indian Constitution (b) VIth Semester: Indian Traditional Knowledge.

(21) The Provisions of Ordinance No. 18 of 2001 in respect of an Ordinance to provide grace marks for passing in a Head of passing and improvement of division (Higher Class) and getting distinction in the subject and condonation of deficiency of marks in a subject in all the Faculties prescribed by the Direction No. 15 of 2017 shall be applicable to each examination under this Direction.

(22) An examinee who does not pass; or who fails to present himself/herself for the examination shall be eligible for re-admission to the same examination/semester, on payment of fresh fees and such other fees as may be prescribed from time to time.

(23) A candidate who could not complete a semester satisfactorily or who has failed will be eligible for readmission to the same semester.
However, re-admission to semester should be allowed only when a regular session is running for the particular semester.

(24) One who has passed the Final B.E./B.Text.E./B.Tech. (Chem. Engg.)/B.Tech. (Chem. Tech.) Polymer (Plastic) Tech. examination of the University in one branch and who desires to take B.E./B.Text.E./B.Tech.(Chem. Engg.)/ B.Tech. (Chem. Tech.) Polymer (Plastic) Tech. Degree in another branch shall be admitted to the third Semester of that branch and shall be governed by this Direction for all other purposes.

(25) After examinations the Board of Examination & Evaluation shall publish the result of the examinees as early as possible and the branch wise merit list shall be notified as per Ordinance No.6.

(26) Notwithstanding anything to the contrary in this Direction, no one shall be admitted to any examination under this Direction, if he/she has already passed the said examinations or an equivalent examinations of any statutory University.

(27) (i) The examinees who have passed in all the subjects prescribed for all the examinations of the particular branch shall be eligible for award of the Degree of Bachelor of Engineering / Bachelor of Technology (Chemical Technology) Polymer (Plastic) in the branch concerned, Bachelor of Textile Engineering and Bachelor of Technology (Chemical Engineering).

(ii) The Degree certificate in the prescribed form shall be signed by the Vice-Chancellor.

(28) The Guidelines of the A.I.C.T.E. New Delhi and D.T.E., Govt. of Maharashtra, Mumbai shall be applicable from time to time after having noted / approved by the Competent Authority.

(29) The existing Direction No. 26/2019 shall stand abrogated stage wise and only applicable to the students who have already sought their admissions as per its provisions and shall abrogated after exhausting the chances given to the failure students of Semester I /II (Group A & B) of B.E. /B.Text. E./B.Tech. (Chem.Engg.) of the University.

(**30**) The provisions in existing Direction Nos. 31/2011, 31/2012, 3/2013, 16/2014, 12/2016, 11/2017 and 37/2018 shall stand only be applicable to the students of Semester III to VIII of the branches Civil Engg., Mechanical Engg., Production Engg., Electronics & Telecommunication Engg., Electronics Engg., Instrumentation Engg., Computer Science & Engg., Computer Engg., Electrical Engg., Electrical Engg. (Electronics & Power), Electrical Engg. (Electrical & Power), Electrical & Electronics Engg., Information Technology, Textile Technology, Chemical Engg., Chemical Technology (Polymer) (Plastic) and Biomedical Engg. who have already sought their admissions as per its provisions and shall stand abrogated after exhausting the chances given to the failure students of Old Course by the University.

Sd/-
Date :- 24/10/2020 (Dr.M. G.Chandekar)
Vice Chancellor

Four Year Degree Course in Bachelor of Engineering Branch : B.E./B.Tech./B.Text. E.(Common to all the Branches) **Appendix-A**
Semester Pattern (Choice Based Credit system)

Sr. No.	Subject Code	Subject	TEACHING SCHEME: HOURS / WEEK Lecture	Tutorial	P/D	Total HOURS/WEEK	CREDITS	EXAMINATION SCHEME: THEORY DURATION OF PAPER (Hr.)	MAX. MARKS THEORY PAPER	MAX. MARKS COLLEGE ASSESMENT	TOTAL	MIN. PASSING MARKS	PRACTICAL MAX. MARKS EXTERNAL	INTERNAL	TOTAL	MIN. PASSING MARKS
Semester :FIRST/ SECOND GROUP A																
THEORY																
01	1 A 1	Engineering Mathematics I	3	1	_	4	4	3	80	20	100	40	_	_	_	_
02	1 A 2	Engineering Physics	4	_	_	4	4	3	80	20	100	40	_	_	_	_
03	1 A 3	Engineering Mechanics	3	1	_	4	4	3	80	20	100	40	_	_	_	_
04	1 A 4	Computer Programming	3	_	_	3	3	3	80	20	100	40	_	_	_	_
PRACTICALS																
05	1 A 5	Workshop Practice	_	_	4	4	2	_	_	_	_	_	25	25	50	25
06	1 A 6	Engineering Physics Laboratory	_	_	2	2	1	_	_	_	_	_	25	25	50	25
07	1 A 7	Engineering Mechanics Laboratory	_	_	2	2	1	_	_	_	_	_	25	25	50	25
08	1 A 8	Computer Programming Laboratory	_	_	2	2	1	_	_	_	_	_	25	25	50	25
		TOTAL	13	2	10	25	20				400				200	
	Note- An Induction Program of Three Weeks duration to be offered to the students at the start of First Year.													TOTAL	600	
Semester :FIRST/ SECOND GROUP B																
THEORY																
01	1 B 1	Engineering Mathematics II	3	1	_	4	4	3	80	20	100	40	_	_	_	_
02	1 B 2	Engineering Chemistry	4	_	_	4	4	3	80	20	100	40	_	_	_	_
03	1 B 3	Basic Electrical Engineering	3	1	_	4	4	3	80	20	100	40	_	_	_	_
04	1 B 4	Engineering Graphics	3	_	_	3	3	3	80	20	100	40	_	_	_	_
PRACTICALS																
05	1 B 5	English Communication Skills Laboratory	_	_	4	4	2	_	_	_	_	_	25	25	50	25
06	1 B 6	Engineering Chemistry Laboratory	_	_	2	2	1	_	_	_	_	_	25	25	50	25
07	1 B 7	Basic Electrical Engineering Laboratory	_	_	2	2	1	_	_	_	_	_	25	25	50	25
08	1 B 8	Engineering Graphics Laboratory	_	_	2	2	1	_	_	_	_	_	25	25	50	25
		TOTAL	13	2	10	25	20				400				200	
														TOTAL	600	

Note- An Induction Program of Three Weeks duration to be offered to the students at the start of First Year.

Appendix – B

The procedure for bifurcation of the students in Group – A and Group-B of First Year Scheme for B.E. / B.Text.E. / B.Tech. (Chem. Engg.) / B.Tech. (Chem. Tech.) Polymer (Plastic) Tech.

1) The sanctioned intake and / or the number of candidates admitted to first year Engineering shall be divided into two groups as A and B in multiples of 60 preferably at the institute level.

2) Group-A candidates shall register for Group-A subjects in first semester and Group-B candidates shall register for Group-B subjects in first semester.

3) The candidates shall be examined for their subjects from the respective groups in first semester.

4) In the Second semester, candidates from Group-B shall register for subject of Group-A. Similarly, candidates from Group-A shall register for subjects of Group-B.

5) The candidates shall be examined for their subjects from the other groups in second semester.

6) Thus, at the end of the first year, all the subjects shall be studied by the candidates from both the groups.

7) The mark list shall show only the group obtained in respective Semester, like First Semester Group- B, First Semester Group-A.

8) The exercise on the part of the college shall be to ensure that the candidates fill up the examination forms correctly according to the subjects group they have registered in both the semesters.

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Four Year Degree Course in Bachelor of Engineering Branch: **ELECTRONICS & TELECOMMUNICATION ENGINEERING**
Semester Pattern (Choice Based Credit Grade System)

SEMESTER : THIRD

Sr. No.	Subject Code	Subject	TEACHING SCHEME					EXAMINATION SCHEME								
			HOURS / WEEK			Total HOURS/WEEK	CREDITS	THEORY					PRACTICAL			
			Lecture	Tutorial	P/D			Duration Of Paper (Hr.)	Max. Marks Theory Paper	Internal Marks	Total	Min. Passing Marks	Max. Marks		Total	Min. Passing Marks
													Int.	Ext.		
THEORY																
01	3ETC01	Engineering Mathematics-III	4	--	--	4	4	3	80	20	100	40	--	--	--	--
02	3ETC02	Electronic Devices & Circuits	3	--	--	3	3	3	80	20	100	40	--	--	--	--
03	3ETC03	Digital System Design	3	--	--	3	3	3	80	20	100	40	--	--	--	--
04	3ETC04	Electromagnetic Waves	3	--	--	3	3	3	80	20	100	40	--	--	--	--
05	3ETC05	Object Oriented Programming (ES)	3	--	--	3	3	3	80	20	100	40	--	--	--	--
06	4ES06	**Environmental Science (Mandatory Course)	2	--	--	2	0	--	--	--	--	--	-	-	-	-
PRACTICALS / DRAWING / DESIGN																
07	3ETC06	Electronic Devices and Circuits Lab	--	--	2	2	1	--	--	--	--	--	25	25	50	25
08	3ETC07	Digital System Design	--	--	2	2	1	--	--	--	--	--	25	25	50	25
09	3ETC08	Object Oriented Programming Lab	--	--	2	2	1	--	--	--	--	--	25	25	50	25
10	3ETC09	Electronic Workshop	--	--	2	2	1	--	--	--	--	--	25	25	50	25
		Total	**18**	**0**	**8**	**26**	**20**	--	--	--	**500**	--	--	--	**200**	--
														Total	**700**	

Note: **The Examination of Mandatory Subject Environmental Science shall be conducted in IV Semester.

SEMESTER : FOURTH

Sr. No.	Subject Code	Subject	TEACHING SCHEME					EXAMINATION SCHEME								
			HOURS / WEEK			Total HOURS/WEEK	CREDITS	THEORY					PRACTICAL			
			Lecture	Tutorial	P/D			Duration Of Paper (Hr.)	Max. Marks Theory Paper	Internal Marks	Total	Min. Passing Marks	Max. Marks Int.	Max. Marks Ext.	Total	Min. Passing Marks
THEORY																
01	4ETC01	Analog and Digital Communication	3	--	--	3	3	3	80	20	100	40	--	--	--	--
02	4ETC02	Analog Circuits	3	--	--	3	3	3	80	20	100	40	--	--	--	--
03	4ETC03	Network Theory	4	--	--	4	4	3	80	20	100	40	--	--	--	--
04	4ETC04	Signals and Systems	3	--	--	3	3	3	80	20	100	40	--	--	--	--
05	4ETC05	Values and Ethics (HS)	3	--	--	3	3	3	80	20	100	40	--	--	--	--
06	4ES06	**Environmental Science (Mandatory Course)	2	--	--	2	2	3	80	20	100	40	-	-	-	-
PRACTICALS / DRAWING / DESIGN																
07	4ETC06	Analog and Digital Communication Lab	--	--	2	2	1	--	--	--	--	--	25	25	50	25
08	4ETC07	Analog Circuits Lab	--	--	2	2	1	--	--	--	--	--	25	25	50	25
09	4ETC08	Network Theory Lab	--	--	2	2	1	--	--	--	--	--	25	25	50	25
10	4ETC09	Signals & Systems Lab	--	--	2	2	1	--	--	--	--	--	25	25	50	25
		Total	**18**	**0**	**8**	**26**	**22**	--	--	--	**600**	--	--	--	**200**	--
														Total	**800**	

Note: **The Examination of Mandatory Subject Environmental Science shall be conducted in IV Semester.

SEMESTER : FIFTH																	
Sr. No.	Subject Code	Subject	TEACHING SCHEME					EXAMINATION SCHEME									
			HOURS / WEEK			Total HOURS/WEEK	CREDITS	THEORY					PRACTICAL				
			Lecture	Tutorial	P/D			Duration Of Paper (Hr.)	Max. Marks Theory Paper	Internal Marks	Total	Min. Passing Marks	Max. Marks Int.	Max. Marks Ext.	Total	Min. Passing Marks
THEORY																	
01	5ETC01	Microcontroller	4	--	--	4	4	3	80	20	100	40	--	--	--	--
02	5ETC02	Control System	3	--	--	3	3	3	80	20	100	40	--	--	--	--
03	5ETC03	Digital Signal Processing	3	--	--	3	3	3	80	20	100	40	--	--	--	--
04	5ETC04	Professional Elective –I (PE-I)	3	--	--	3	3	3	80	20	100	40	--	--	--	--
05	5ETC05	Open Elective – I (OE-I)	3	--	--	3	3	3	80	20	100	40	--	--	--	--
PRACTICALS / DRAWING / DESIGN																	
06	5ETC06	Microcontroller Lab	--	--	2	2	1	--	--	--	--	--	25	25	50	25
07	5ETC07	Digital Signal Processing Lab	--	--	2	2	1	--	--	--	--	--	25	25	50	25
08	5ETC08	Power Electronics Lab	--	--	2	2	1	--	--	--	--	--	25	25	50	25
09	5ETC09	Electronic lab based on Instrumentation	--	--	2	2	1	--	--	--	--	--	25	25	50	25
		Total	**16**	**0**	**8**	**24**	**20**	--	--	--	**500**	--	--	--	**200**	--
														Total	**700**	

5ETC04: PE (I) : (i) Power Electronics (ii) Fiber Optic Communication (iii) Speech and Audio Processing

5ETC05: OE (I) : (i) Sensors and Transducers (ii) Data Structure (iii) Introduction to Java

A student will be eligible to get Under Graduate degree with Honors or additional Minor Engineering, if he/she completes an additional 20 credits relevant to the UG program.
The detail of which is as follows:

Course Name	Semester	Credit
MOOCs Course-I	**V**	**04**
MOOCs Course-II	**VI**	**04**
MOOCs Course-III	**VII**	**04**
MOOCs Course-IV	**VIII**	**04**
Internship	**V to VIII Sem**	**02**
Industrial Visit	**V to VIII Sem**	**02**
	Total	**20**

Note: The student needs to submit
1. **MOOCs Course passing certificate of each semester**
2. **Completion & Evaluation Certificate of Internship**
3. **Industrial Visit certificate.**

Note: Only One MOOCs course per semester shall be considered.

SEMESTER : SIXTH

Sr. No.	Subject Code	Subject	TEACHING SCHEME					EXAMINATION SCHEME								
			HOURS / WEEK			Total HOURS/WEEK	CREDITS	THEORY					PRACTICAL			
			Lecture	Tutorial	P/D			Duration Of Paper (Hr.)	Max. Marks Theory Paper	Internal Marks	Total	Min. Passing Marks	Max. Marks		Total	Min. Passing Marks
													Int.	Ext.		
THEORY																
01	6ETC01	Communication Network	3	--	--	3	3	3	80	20	100	40	--	--	--	--
02	6ETC02	Computer Architecture	4	--	--	4	4	3	80	20	100	40	--	--	--	--
03	6ETC03	Professional Elective -II (PE-II)	3	--	--	3	3	3	80	20	100	40	--	--	--	--
04	6ETC04	Open Elective - II (OE-II)	3	--	--	3	3	3	80	20	100	40	--	--	--	--
05	6ETC05	Economics for Engineers (HS)	3	--	--	3	3	3	80	20	100	40	--	--	--	--
PRACTICALS / DRAWING / DESIGN																
06	6ETC06	Communication Network Lab	--	--	2	2	1	--	--	--	--	--	25	25	50	25
07	6ETC07	Electronic Circuit Design Lab (Hardware + Software)	--	--	2	2	1	--	--	--	--	--	25	25	50	25
08	6ETC08	Python Programming Lab	--	--	2	2	1	--	--	--	--	--	25	25	50	25
09	6ETC09	Mini Project	--	--	2	2	1	--	--	--	--	--	50	--	50	25
		Total	**16**	**0**	**8**	**24**	**20**	--	--	--	**500**	--	--	--	**200**	--
														Total	**700**	

6ETC03: PE (II) : (i) CMOS Design (ii) Satellite Communication (iii) Adaptive Signal Processing

6ETC04: OE (II) : (i) Introduction to Python Programming (ii) Data Base Management System
(iii) Renewable Energy Sources (Solar & Electric Vehicles)

SEMESTER : SEVENTH

Sr. No.	Subject Code	Subject	TEACHING SCHEME					EXAMINATION SCHEME								
			HOURS / WEEK			Total HOURS/WEEK	CREDITS	THEORY					PRACTICAL			
			Lecture	Tutorial	P/D			Duration Of Paper (Hr.)	Max. Marks Theory Paper	Internal Marks	Total	Min. Passing Marks	Max. Marks		Total	Min. Passing Marks
													Int.	Ext.		
THEORY																
01	7ETC01	Microwave Theory and Techniques	3	--	--	3	3	3	80	20	100	40	--	--	--	--
02	7ETC02	Digital Image and Video Processing	3	--	--	3	3	3	80	20	100	40	--	--	--	--
03	7ETC03	Project Management and Entrepreneurship	3	--	--	3	3	3	80	20	100	40	--	--	--	--
04	7ETC04	Professional Elective - III (PE-III)	3	--	--	3	3	3	80	20	100	40	--	--	--	--
05	7ETC05	Professional Elective- IV (PE-IV)	3	--	--	3	3	3	80	20	100	40	--	--	--	--
PRACTICALS / DRAWING / DESIGN																
06	7ETC06	Microwave Theory and Techniques Lab	--	--	2	2	1	--	--	--	--	--	25	25	50	25
07	7ETC07	Digital Image and Video Processing Lab	--	--	2	2	1	--	--	--	--	--	25	25	50	25
08	7ETC08	Project Management and Entrepreneurship Lab	--	--	2	2	1	--	--	--	--	--	25	25	50	25
09	7ETC09	** Project Stage I (Seminar)	--	--	8	8	4	--	--	--	--	--	100	--	100	50
		Total	**15**	**0**	**14**	**29**	**22**	--	--	--	**500**	--	--	--	**250**	--
														Total	**750**	

7ETC04: PE(III) : (i) High Speed Electronics (ii) Mobile Communication and Networks (iii) Mixed Signal Design

7ETC05: PE(IV) : (i) Introduction to MEMS (ii)Error Correcting Codes(iii) Antenna and Propagation

Note: ** Seminar based on Final year Major Project

SEMESTER : EIGHT

Sr. No.	Subject Code	Subject	TEACHING SCHEME					EXAMINATION SCHEME								
			HOURS / WEEK			Total HOURS/WEEK	CREDITS	THEORY					PRACTICAL			
			Lecture	Tutorial	P/D			Duration Of Paper (Hr.)	Max. Marks Theory Paper	Internal Marks	Total	Min. Passing Marks	Max. Marks		Total	Min. Passing Marks
													Int.	Ext.		
THEORY																
01	8ETC01	Embedded Systems	3	--		3	3	3	80	20	100	40	--	--	--	--
02	8ETC02	Cryptography & Network security	3	--		3	3	3	80	20	100	40	--	--	--	--
03	8ETC03	Prof. Elective-V (PE-V)	3	--		3	3	3	80	20	100	40	--	--	--	--
04	8ETC04	Prof. Elective-VI (PE-VI)	3	--		3	3	3	80	20	100	40	--	--	--	--
PRACTICALS / DRAWING / DESIGN																
05	8ETC05	Embedded Systems- Lab	--	--	2	2	1	--	--	-- --	--	--	25	25	50	25
06	8ETC06	Cryptography & Network security Lab	--	--	2	2	1	--	--	-- --	--	--	25	25	50	25
07	8ETC07	Project stage -II	--	--	12	12	6	--	--	--	--	--	100	100	200	100
		Total	**12**	**--**	**16**	**28**	**20**	**--**	**--**	**--**	**400**	**--**	**--**	**--**	**300**	--
														Total	**700**	

8ETC03 : PE-V: (i) Nano Electronics (ii) Wireless Sensor Networks (iii) Wavelets (iv) Bio-medical Electronics

8ETC04 : PE-VI: (i) 5G-6G Mobile Communication (ii)Information Theory & Coding (iii) Scientific Computing

Four Year Degree Course in Bachelor of Engineering Branch: **COMPUTER SCIENCE & ENGINEERING**

Semester Pattern (Choice Based Credit Grade System)

SEMESTER : THIRD

Sr. No.	Subject Code	Subject	TEACHING SCHEME					EXAMINATION SCHEME								
			HOURS / WEEK			Total HOURS/WEEK	CREDITS	THEORY					PRACTICAL			
			Lecture	Tutorial	P/D			Duration Of Paper (Hr.)	Max. Marks Theory Paper	Internal Marks	Total	Min. Passing Marks	Max. Marks		Total	Min. Passing Marks
													Int.	Ext.		
THEORY																
01	3KS01	Mathematics-III	3	1	--	4	4	3	80	20	100	40	--	--	--	--
02	3KS02	Discrete Structure & Graph Theory	3	--	--	3	3	3	80	20	100	40	--	--	--	--
03	3KS03	Object Oriented Programming	3	--	--	3	3	3	80	20	100	40	--	--	--	--
04	3KS04	Data Structures	3	--	--	3	3	3	80	20	100	40	--	--	--	--
05	3KS05	Analog & Digital Electronics	3	--	--	3	3	3	80	20	100	40	--	--	--	--
06	4ES06	Environmental Studies *	2	--	--	2	0	--	--	--	--	--	-	-	-	-
PRACTICALS / DRAWING / DESIGN																
07	3KS06	Object Oriented Programming Jawa-Lab	--	--	2	2	1	--	--	--	--	--	25	25	50	25
08	3KS07	Data Structures Lab	--	--	2	2	1	--	--	--	--	--	25	25	50	25
09	3KS08	Analog & Digital Electronics Lab	--	--	2	2	1	--	--	--	--	--	25	25	50	25
10	3KS09	C Skill-Lab I (#)	--	--	2	2	1	--	--	--	--	--	25	25	50	25
		Total	**17**	**1**	**8**	**26**	**20**	--	--	--	**500**	--	--	--	**200**	--
														Total	**700**	

Note: **The Examination of the Subject Environmental Science shall be conducted in IV Semester as per Ordinance No. 42 of 2005.

C Skill Lab I - based on technology like -**Python/Django** etc. to be decided by Individual Dept. of respective College.

SEMESTER : FOURTH

Sr. No.	Subject Code	Subject	TEACHING SCHEME					EXAMINATION SCHEME								
			HOURS / WEEK			Total HOURS/WEEK	CREDITS	THEORY					PRACTICAL			
			Lecture	Tutorial	P/D			Duration Of Paper (Hr.)	Max. Marks Theory Paper	Internal Marks	Total	Min. Passing Marks	Max. Marks Int.	Max. Marks Ext.	Total	Min. Passing Marks
THEORY																
01	4KS01	Artificial Intelligence	3	--	--	3	3	3	80	20	100	40	--	--	--	--
02	4KS02	Data Communication & Networking	3	--	--	3	3	3	80	20	100	40	--	--	--	--
03	4KS03	Operating System	3	--	--	3	3	3	80	20	100	40	--	--	--	--
04	4KS04	Microprocessor & Assembly Lang. Prog.	3	--	--	3	3	3	80	20	100	40	--	--	--	--
05	4KS05	Theory of Computation	3	1	--	4	4	3	80	20	100	40	--	--	--	--
06	4ES06	Environmental Studies *	2	--	--	2	2	3	80	20	100	40	-	-	-	-
PRACTICALS / DRAWING / DESIGN																
07	4KS06	Data Communication & Networking Lab	--	--	2	2	1	--	--	--	--	--	25	25	50	25
08	4KS07	Operating System Lab	--	--	2	2	1	--	--	--	--	--	25	25	50	25
09	4KS08	Microprocessor & Assembly Lang. Prog. Lab	--	--	2	2	1	--	--	--	--	--	25	25	50	25
10	4KS09	C Skill-Lab II (#)	--	--	2	2	1	--	--	--	--	--	25	25	50	25
		Total	**17**	**1**	**8**	**26**	**22**	--	--	--	**600**	--	--	--	**200**	--
														Total	**800**	

Note: **The Examination of Mandatory Subject Environmental Science shall be conducted in IV Semester.

C Skill Lab II - based on technology like -**PHP, Web Technology, Raspberry Pi/Ardino**, etc. to be decided by Individual Dept. of respective College.

SEMESTER : FIFTH

Sr. No.	Subject Code	Subject	TEACHING SCHEME					EXAMINATION SCHEME								
			HOURS / WEEK			Total HOURS/WEEK	CREDITS	THEORY					PRACTICAL			
			Lecture	Tutorial	P/D			Duration Of Paper (Hr.)	Max. Marks Theory Paper	Internal Marks	Total	Min. Passing Marks	Max. Marks		Total	Min. Passing Marks
													Int.	Ext.		
THEORY																
01	5KS01	Database Management Systems	4	--	--	4	4	3	80	20	100	40	--	--	--	--
02	5KS02	Compiler Design	3	--	--	3	3	3	80	20	100	40	--	--	--	--
03	5KS03	Computer Architecture & Organization	3	--	--	3	3	3	80	20	100	40	--	--	--	--
04	5KS04	Professional Elective –I (PE-I) *	3	--	--	3	3	3	80	20	100	40	--	--	--	--
05	5KS05	Open Elective – I (OE-I) **	3	--	--	3	3	3	80	20	100	40	--	--	--	--
PRACTICALS / DRAWING / DESIGN																
06	5KS06	Database Management Systems - Lab (@)	--	--	2	2	1	--	--	--	--	--	25	25	50	25
07	5KS07	Compiler Design Lab	--	--	2	2	1	--	--	--	--	--	25	25	50	25
08	5KS08	Emerging Tech. Lab-I	--	--	2	2	1	--	--	--	--	--	25	25	50	25
09	5KS09	C Skill Lab III (*)	--	--	2	2	1	--	--	--	--	--	25	25	50	25
		Total	**16**	**0**	**8**	**24**	**20**	--	--	--	**500**	--	--	--	**200**	--
														Total	**700**	

Prof. Elect I (*) : i) Cognitive Technologies
(ii) Data Science and Statistics
(iii) Internet of Things
(iv) Introduction to Cyber Security

Open Elect : I (**) (i) Fund. of Fin. & Acctg.
(ii) Prin. of Marketing for Engg.
(iii) Entrepreneurship

* **C Skill Lab III** - based on technology like - **Angular & React, Express, Node.js** etc.
to be decided by Individual Dept. of respective College

(@ Practicals using Mongo DB,MySQL

Emerging Technology Lab# I : AI : IBM Watson, Microsoft Cognitive Toolkit , Tensor Flow, Apache System ML, Caffe, Open NN, Torch, Neuroph
DS : R, Python, Cassandra, Apache Hadoop
IoT : Arduino, DeviceHive, Kaa, Home Assistant
CS : Kali Linux, Open VPN, NMAP, Metasploit Framework

An Orientation Program of 15 hours duration /MOOC on <u>Indian Constitution</u> to be offered to the students during the Vth Semester

Open Elective I to be opted from the courses offered by other engineering technology boards of the university /Massive Open learning Courses (MOOC) such as SWAYAM pertaining to the profession

SEMESTER : SIXTH

Sr. No.	Subject Code	Subject	TEACHING SCHEME					EXAMINATION SCHEME								
			HOURS / WEEK			Total HOURS/WEEK	CREDITS	THEORY					PRACTICAL			
			Lecture	Tutorial	P/D			Duration Of Paper (Hr.)	Max. Marks Theory Paper	Internal Marks	Total	Min. Passing Marks	Max. Marks Int.	Max. Marks Ext.	Total	Min. Passing Marks
THEORY																
01	6KS01	Security Policy & Governance	3	--	--	3	3	3	80	20	100	40	--	--	--	--
02	6KS02	Design & Analysis of Algorithms	4	--	--	4	4	3	80	20	100	40	--	--	--	--
03	6KS03	Software Engg.	3	--	--	3	3	3	80	20	100	40	--	--	--	--
04	6KS04	Prof. Elective -II (PE-II)	3	--	--	3	3	3	80	20	100	40	--	--	--	--
05	6KS05	Open Elective - II (OE-II)	3	--	--	3	3	3	80	20	100	40	--	--	--	--
PRACTICALS / DRAWING / DESIGN																
06	6KS06	Design & Analysis of Algorithms- Lab.	--	--	2	2	1	--	--	--	--	--	25	25	50	25
07	6KS07	Software Engg. – lab.	--	--	2	2	1	--	--	--	--	--	25	25	50	25
08	6KS08	Emerging Tech. Lab-II	--	--	2	2	1	--	--	--	--	--	25	25	50	25
09	6KS09	C Skill Lab IV (*)	--	--	2	2	1	--	--	--	--	--	25	25	50	25
		Total	**16**	**0**	**8**	**24**	**20**	--	--	--	**500**	--	--	--	**200**	--
														Total	**700**	

Prof. Elect II (*) : i) Natural Language Processing
(ii) Big Data Analytics
(iii) Sensors & Actuators
iv) Cryptography

Open Elect : II (**) (i) Computational Biology
(ii) Cyber Law & Ethics
(iii) Intellectual Property Right

FOSS Tools & Technology for Practicals :
Natural Language Toolkit (NLTK),SpaCy, PyTorch-NLP, Natural, Retext, Text Blob
KNIME, Spark, Neo4J, MongoDB, Hive, Storm
Devicehub, Zetta, Node-RED, Flutter, M2MLabs Mainspring
VeraCrypt, ModSecurity, AdBlocker, CheckShortURL, SPAMfighter, SpamBully

* C Skill Lab IV - based on technology like - **DevOp to be decided by Individual Dept. of respective College**

An Orientation Program of 15 hours duration /MOOC on* Indian Constitution *to be offered to the students during the Vth Semester .

Open Elective II to be opted from the courses offered by other engineering technology boards of the university /Massive Open learning Courses (MOOC) such as SWAYAM pertaining to the profession

SEMESTER : SEVENTH																
Sr. No.	Subject Code	Subject	TEACHING SCHEME					EXAMINATION SCHEME								
			HOURS / WEEK			Total HOURS/WEEK	CREDITS	THEORY					PRACTICAL			
			Lecture	Tutorial	P/D			Duration Of Paper (Hr.)	Max. Marks Theory Paper	Internal Marks	Total	Min. Passing Marks	Max. Marks		Total	Min. Passing Marks
													Int.	Ext.		
THEORY																
01	7KS01	Social Science & Engineering Economics	3	--	--	3	3	3	80	20	100	40	--	--	--	--
02	7KS02	Computer Graphics	3	--	--	3	3	3	80	20	100	40	--	--	--	--
03	7KS03	Cloud Computing	4	--	--	4	4	3	80	20	100	40	--	--	--	--
04	7KS04	Prof. Elective - III (PE-III) (*)	3	--	--	3	3	3	80	20	100	40	--	--	--	--
05	7KS05	Prof. Elect.- IV (PE-IV) (**)	3	--	--	3	3	3	80	20	100	40	--	--	--	--
PRACTICALS / DRAWING / DESIGN																
06	7KS06	Computer Graphics- Lab.	--	--	2	2	1	--	--	--	--	--	25	25	50	25
07	7KS07	Emerging Tech. Lab-III	--	--	2	2	1	--	--	--	--	--	25	25	50	25
08	7KS08	Emerging Tech. Lab-IV	--	--	2	2	1	--	--	--	--	--	25	25	50	25
09	7KS09	** Project & Seminar	--	--	8	8	4	--	--	--	--	--	--	50	50	25
		Total	**16**	**0**	**14**	**30**	**23**	--	--	--	**500**	--	--	--	**200**	--
														Total	**700**	

Prof. Elect III (*) : (i) Robotics
(ii) Data Warehousing & Mining
(iii) Embedded Systems
iv) Digital Forensic

Prof. Elect : IV (**) (i) Block Chain Fundamentals
(ii) Image Processing
(iii) Optimization Techniques

Emerging Technology Lab# V : Ethereum,Bigchain DB, Corda
OpenCV, Simple CV, Keras, Caffe
Open Eaagles, Repast, Open Simulator

SEMESTER : EIGHT																
Sr. No.	**Subject Code**	**Subject**	**TEACHING SCHEME**					**EXAMINATION SCHEME**								
			HOURS / WEEK			**Total HOURS/WEEK**	**CREDITS**	**THEORY**					**PRACTICAL**			
			Lecture	**Tutorial**	**P/D**			**Duration Of Paper (Hr.)**	**Max. Marks Theory Paper**	**Internal Marks**	**Total**	**Min. Passing Marks**	**Max. Marks**		**Total**	**Min. Passing Marks**
													Int.	**Ext.**		
THEORY																
01	8KS01	Object Oriented Analysis & Design	3	--		3	3	3	80	20	100	40	--	--	--	--
02	8KS02	Professional Ethics & Management	3	--		3	3	3	80	20	100	40	--	--	--	--
03	8KS03	Prof. Elective-V (PE-V)	3	--		3	3	3	80	20	100	40	--	--	--	--
04	8KS04	Prof. Elective-VI (PE-VI)	3	--		3	3	3	80	20	100	40	--	--	--	--
PRACTICALS / DRAWING / DESIGN																
05	8KS05	Emerging Tech. Lab-V	--	--	2	2	1	--	--	-- --	--	--	25	25	50	25
06	8KS02	Emerging Tech. Lab-VI	--	--	2	2	1	--	--	-- --	--	--	25	25	50	25
07	8KS03	Project & Seminar	--	--	12	12	6	--	--	--	--	--	75	75	150	75
		Total	**12**	**--**	**16**	**28**	**20**	**--**	**--**	**--**	**400**	**--**	**--**	**--**	**250**	--
														Total	**650**	

Prof. Elect V (*) : (i) Virtual & Augmented Reality
(ii) Machine Learning and AI
(iii) Wireless Sensor Networks
iv) System & Software Security

Prof. Elect : VI (**) (i) Distributed Ledger Technology
(ii) Multimedia Computing
(iii) Modeling & Simulation

Emerging Tech. Lab# V : i) Google's ARCore, AR.js, ARToolKit, , DroidAR Brio, Adobe Aero
ii) R Studio, Orange, D3.js, Ggplot2, Jupyter Notebooks
iii) Wireshark, Burp Suit, Nessus

Emerging Tech. Lab# VI : i) Hyperledger, HydraChain, MultiChain, Elements
ii) Google Colab, GPUImage, Cuda, Aforge/Accord.NET
iii) OR-Tools, Locust.io, httperf, Apache JMeter, Siege

Four Year Degree Course in Bachelor of Engineering Branch: **INFORMATION TECHNOLOGY**
Semester Pattern (Choice Based Credit Grade System)

SEMESTER : THIRD																
Sr. No.	Subject Code	Subject	TEACHING SCHEME					EXAMINATION SCHEME								
			HOURS / WEEK			Total HOURS/WEEK	CREDITS	THEORY					PRACTICAL			
			Lecture	Tutorial	P/D			Duration Of Paper (Hr.)	Max. Marks Theory Paper	Internal Marks	Total	Min. Passing Marks	Max. Marks		Total	Min. Passing Marks
													Int.	Ext.		
THEORY																
01	3IT01	Mathematics-III	3	1	--	4	4	3	80	20	100	40	--	--	--	--
02	3IT02	Discrete Structure & Graph Theory	3	--	--	3	3	3	80	20	100	40	--	--	--	--
03	3IT03	Object Oriented Programming	3	--	--	3	3	3	80	20	100	40	--	--	--	--
04	3IT04	Assembly Language Programming	3	--	--	3	3	3	80	20	100	40	--	--	--	--
05	3IT05	Analog & Digital Electronics	3	--	--	3	3	3	80	20	100	40	--	--	--	--
06	4ES06	**Environmental Studies	2	--	--	2	0	--	--	--	--	--	-	-	-	-
PRACTICALS / DRAWING / DESIGN																
07	3IT06	Object Oriented Programming Jawa lab.	--	--	2	2	1	--	--	--	--	--	25	25	50	25
08	3IT07	Assembly Language Programming- Lab.	--	--	2	2	1	--	--	--	--	--	25	25	50	25
09	3IT08	Analog & Digital Electronics- Lab.	--	--	2	2	1	--	--	--	--	--	25	25	50	25
10	3IT09	Comp. Skil Lab.-I	--	--	2	2	1	--	--	--	--	--	25	25	50	25
		Total	**17**	**1**	**8**	**26**	**20**	--	--	--	**500**	--	--	--	**200**	--
														Total	**700**	

Note: **(i) The Examination of Mandatory Subject Environmental Science shall be conducted in IV Semester.
(ii) # C Skill Lab I – based on technology like – Python, R etc. to be decided by individual Dept. of respective College.

SEMESTER : FOURTH																	
Sr. No.	Subject Code	Subject	TEACHING SCHEME					EXAMINATION SCHEME									
			HOURS / WEEK			Total HOURS/WEEK	CREDITS	THEORY					PRACTICAL				
			Lecture	Tutorial	P/D			Duration Of Paper (Hr.)	Max. Marks Theory Paper	Internal Marks	Total	Min. Passing Marks	Max. Marks		Total	Min. Passing Marks
													Int.	Ext.		
THEORY																	
01	4IT01	Computer Organization & Architecture	3	1	--	4	4	3	80	20	100	40	--	--	--	--
02	4IT02	Data Communication & Networking	3	--	--	3	3	3	80	20	100	40	--	--	--	--
03	4IT03	Operating System	3	--	--	3	3	3	80	20	100	40	--	--	--	--
04	4IT04	Data Structures	3	--	--	3	3	3	80	20	100	40	--	--	--	--
05	4IT05	Social Science & Engg. Economics	3	--	--	3	3	3	80	20	100	40	--	--	--	--
06	4ES06	**Environmental Science	2	--	--	2	2	3	80	20	100	40	-	-	-	-
PRACTICALS / DRAWING / DESIGN																	
07	4IT06	Data Communication & Networking Lab	--	--	2	2	1	--	--	--	--	--	25	25	50	25
08	4IT07	Operating System Lab	--	--	2	2	1	--	--	--	--	--	25	25	50	25
09	4IT08	Data Structures Lab	--	--	2	2	1	--	--	--	--	--	25	25	50	25
10	4IT09	Comp. Skill Lab.-II	--	--	2	2	1	--	--	--	--	--	25	25	50	25
		Total	**17**	**1**	**8**	**26**	**22**	--	--	--	**600**	--	--	--	**200**	--
														Total	**800**	

Note: **(i)The Examination of Mandatory Subject Environmental Science shall be conducted in IV Semester.
(ii) # C Skill Lab I – based on technology like – Python, R etc. to be decided by individual Dept. of respective College.

SEMESTER : FIFTH																
Sr. No.	Subject Code	Subject	TEACHING SCHEME					EXAMINATION SCHEME								
			HOURS / WEEK			Total HOURS/WEEK	CREDITS	THEORY					PRACTICAL			
			Lecture	Tutorial	P/D			Duration Of Paper (Hr.)	Max. Marks Theory Paper	Internal Marks	Total	Min. Passing Marks	Max. Marks Int.	Max. Marks Ext.	Total	Min. Passing Marks
THEORY																
01	5IT01	Database Management Systems	4	--	--	4	4	3	80	20	100	40	--	--	--	--
02	5IT02	Theory of Computation	3	--	--	3	3	3	80	20	100	40	--	--	--	--
03	5IT03	Software Engineering	3	--	--	3	3	3	80	20	100	40	--	--	--	--
04	5IT04	Professional Elective –I (PE-I)	3	--	--	3	3	3	80	20	100	40	--	--	--	--
05	5IT05	Open Elective – I (OE-I)	3	--	--	3	3	3	80	20	100	40	--	--	--	--
PRACTICALS / DRAWING / DESIGN																
06	5IT06	Database Management Systems Lab	--	--	2	2	1	--	--	--	--	--	25	25	50	25
07	5IT07	Software Engineering Lab	--	--	2	2	1	--	--	--	--	--	25	25	50	25
08	5IT08	Professional Elective –I Lab	--	--	2	2	1	--	--	--	--	--	25	25	50	25
09	5IT09	Comp. Skill Lab.-III (#)	--	--	2	2	1	--	--	--	--	--	25	25	50	25
		Total	**16**	**0**	**8**	**24**	**20**	--	--	--	**500**	--	--	--	**200**	--
														Total	**700**	

5IT04: PE (I) : (i) Information Security Systems (ii) Data Science & Statistics (iii) Internet of Things

5IT05: OE (I) : (i) Soft Skills & Interpersonal Communication (ii) Computational Biology (iii) Cyber Law & Ethics. Open Elective- I to be offered from the Courses offered by other Engg. & Technology Boards of the University / Massive Open Learning Courses (MOOCs) such as SWAYAM pertaining to the profession.

(#) Computer Skill Lab III-based on technology like-DevOp, Angular & React, etc. to be decided by Individual Dept. of respective College.

An Orientation Program of 15 hours duration / MOOCs on **Indian Constitution** to be offered to the students during the **V th Semester.**

SEMESTER : SIXTH

Sr. No.	Subject Code	Subject	TEACHING SCHEME					EXAMINATION SCHEME								
			HOURS / WEEK			Total HOURS/WEEK	CREDITS	THEORY					PRACTICAL			
			Lecture	Tutorial	P/D			Duration Of Paper (Hr.)	Max. Marks Theory Paper	Internal Marks	Total	Min. Passing Marks	Max. Marks Int.	Max. Marks Ext.	Total	Min. Passing Marks
THEORY																
01	6IT01	Compiler Design	4	--	--	4	4	3	80	20	100	40	--	--	--	--
02	6IT02	Design & Analysis of Algorithms	3	--	--	3	3	3	80	20	100	40	--	--	--	--
03	6IT03	Artificial Intelligence	3	--	--	3	3	3	80	20	100	40	--	--	--	--
04	6IT04	Prof. Elective - II (PE-II)	3	--	--	3	3	3	80	20	100	40	--	--	--	--
05	6IT05	Open Elective - II (OE-II)	3	--	--	3	3	3	80	20	100	40	--	--	--	--
PRACTICALS / DRAWING / DESIGN																
06	6IT06	Compiler Design Lab	--	--	2	2	1	--	--	--	--	--	25	25	50	25
07	6IT07	Design & Analysis of Algorithms - Lab	--	--	2	2	1	--	--	--	--	--	25	25	50	25
08	6IT08	Prof. Elective - II - Lab	--	--	2	2	1	--	--	--	--	--	25	25	50	25
09	6IT09	Comp. Skill Lab.-IV (#)	--	--	2	2	1	--	--	--	--	--	50	--	50	25
		Total	**16**	**0**	**8**	**24**	**20**	--	--	--	**500**	--	--	--	**200**	--
														Total	**700**	

6IT04: PE (II) : (i) Cryptography & Network Security (ii) Big Data Analytics (iii) sensors & Activators

6IT05: OE (II) : (i) Economic Policy in India (ii) Human Resource Development & organization (iii) Intellectual Property Right. Open Elective- I to be offered from the Courses offered by other Engg. & Technology Boards of the University / Massive Open Learning Courses (MOOCs) such as SWAYAM pertaining to the profession.

(#) C Skill Lab IV- Mini project based on Software Engineering to be decided by Individual Dept. of the respective College.
An Orientation Programm of 15 hours duration .MOOC on Indian Traditional Knowledge to be offered to the students during the VII Semester.

SEMESTER : SEVENTH

Sr. No.	Subject Code	Subject	TEACHING SCHEME					EXAMINATION SCHEME								
			HOURS / WEEK			Total HOURS/WEEK	CREDITS	THEORY					PRACTICAL			
			Lecture	Tutorial	P/D			Duration Of Paper (Hr.)	Max. Marks Theory Paper	Internal Marks	Total	Min. Passing Marks	Max. Marks		Total	Min. Passing Marks
													Int.	Ext.		
THEORY																
01	7IT01	Mobile Computing	3	--	--	3	3	3	80	20	100	40	--	--	--	--
02	7IT02	Embedded Systems	3	--	--	3	3	3	80	20	100	40	--	--	--	--
03	7IT03	Cloud Computing	3	--	--	3	3	3	80	20	100	40	--	--	--	--
04	7IT04	Prof. Elective - III (PE-III)	3	--	--	3	3	3	80	20	100	40	--	--	--	--
05	7IT05	Prof. Elective- IV (PE-IV)	3	--	--	3	3	3	80	20	100	40	--	--	--	--
PRACTICALS / DRAWING / DESIGN																
06	7IT06	Embedded Systems - Lab	--	--	2	2	1	--	--	--	--	--	25	25	50	25
07	7IT07	Prof. Elective - III Lab	--	--	2	2	1	--	--	--	--	--	25	25	50	25
08	7IT08	Prof. Elective- IV Lab	--	--	2	2	1	--	--	--	--	--	25	25	50	25
09	7IT09	Project & Seminar	--	--	8	8	4	--	--	--	--	--	--	50	50	25
		Total	**15**	**0**	**14**	**29**	**22**	**--**	**--**	**--**	**500**	**--**	**--**	**--**	**200**	**--**
														Total	**700**	

7IT04: PE(III) : (i) Machine learning (ii) Data Warehousing &Mining (iii) Wireless Sensor Networks

7IT05: PE(IV) : (i) Block Chain Fundamentals (ii)Business Intelligence (iii) Digital Forensic

SEMESTER : EIGHT

Sr. No.	Subject Code	Subject	TEACHING SCHEME					EXAMINATION SCHEME								
			HOURS / WEEK			Total HOURS/WEEK	CREDITS	THEORY					PRACTICAL			
								Duration Of Paper (Hr.)	Max. Marks Theory Paper	Internal Marks	Total	Min. Passing Marks	Max. Marks		Total	Min. Passing Marks
			Lecture	Tutorial	P/D								Int.	Ext.		
THEORY																
01	8IT01	Object Oriented Analysis & Design	3	--		3	3	3	80	20	100	40	--	--	--	--
02	8IT02	Professional Ethics & Management	3	--		3	3	3	80	20	100	40	--	--	--	--
03	8IT03	Entrepreneurship & Project Management	3	--		3	3	3	80	20	100	40	--	--	--	--
04	8IT04	Prof. Elective-V (PE-V)	3	--		3	3	3	80	20	100	40	--	--	--	--
PRACTICALS / DRAWING / DESIGN																
05	8IT05	Object Oriented Analysis & Design Lab	--	--	2	2	1	--	--	-- --	--	--	25	25	50	25
06	8IT06	Prof. Elective-V (PE-V)- Lab	--	--	2	2	1	--	--	-- --	--	--	25	25	50	25
07	8IT07	Project & Seminar	--	--	12	12	6	--	--	--	--	--	75	75	150	75
		Total	**12**	**--**	**16**	**28**	**20**	**--**	**--**	**--**	**400**	**--**	**--**	**--**	**250**	**--**
														Total		**650**

8IT04 : PE-V: (i) Robotics (ii) Virtual & Augmented Reality (iii) Human Computer Interaction (iv) Cross Platform Application Development

L : Theory Lecture
T : Tutorial
P : Practical
D : Drawing / Design

FOUR YEAR DEGREE COURSE IN BACHELOR OF TECHNOLOGY
BRANCH: CHEMICAL ENGINEERING
CREDIT GRADE SYSTEM
SEMESTER PATTERN
SEMESTER : THIRD

Sr. No.	Category	Subject Code	Subject	Teaching Scheme					Examination Scheme								
				L	T	P/ D	Total Hours/ week	Credits	Duration of Papers (Hrs.)	Maximum Marks		Total	Min. Pass Marks	Max. Marks Practical		Total Marks	Maximum Passing Marks
										Theory Paper	College Assessment			External	Internal		
1	Basic Science Course	3CH01	Applied Maths-III	3	1	-	4	**4**	3	80	20	100	40	---	---	---	---
2	Professional Core Course	3CH02	Process Instrumentation	3	-	-	3	**3**	3	80	20	100	40	---	---	---	---
3	Professional Core Course	3 CH 03	Strength of Material	3	-	-	3	**3**	3	80	20	100	40	---	---	---	---
4	Professional Core Course	3 CH04	Chemical Engg. Thermodynamics -I	3	-	-	3	**3**	3	80	20	100	40	---	---	---	---
5	Professional Core Course	3CH05	Process Calculation	3	1	-	4	**4**	3	80	20	100	40	---	---	---	---
6	Humanities & Social Science	3ES06	Environmental Studies	2	-	-	2	**0**	---	---	---	---	---	---	---	---	---
7	Professional Core Course	3CH07	Process Instrumentation- Lab	-	-	2	2	**1**	---	---	---	---	---	25	25	50	25
8	Professional Core Course	3CH08	Strength of Material- Lab	-	-	2	2	**1**	---	---	---	---	---	25	25	50	25
9	Professional Core Course	3CH09	Chem. Engg. Thermo-I .-Lab	-	-	2	2	**1**	---	---	---	---	---	25	25	50	25
Total				**17**	**2**	**6**	**25**	**20**				500				150	
Note – Environmental Science as per Ordinance no. 42/2005										**Grand Total**		500				150	**650**

L : Theory Lecture
T : Tutorial
P : Practical
D : Drawing / Design

FOUR YEAR DEGREE COURSE IN BACHELOR OF TECHNOLOGY
BRANCH: CHEMICAL ENGINEERING
CREDIT GRADE SYSTEM
SEMESTER PATTERN
SEMESTER : FOURTH

Sr. No	Category	Subject Code	Subject	Teaching Scheme					Examination Scheme								
				L	T	P/D	Total Hours/week	Credits	Duration of Papers (Hrs.)	Maximum Marks		Total	Min. Pass Marks	Max. Marks Practical		Total Marks	Maximum Passing Marks
										Theory Paper	College Assessment			External	Internal		
1	Engineering Science Course	4CH01	Applied Physical Chemistry	3	-	-	3	3	3	80	20	100	40	---	---	---	---
2	Engineering Science Course	4CH02	Machine Design & Drawing	3	-	-	3	3	3	80	20	100	40	---	---	---	---
3	Professional Core Course	4CH03	Fluid Flow Operation	3	-	-	3	3	3	80	20	100	40	---	---	---	---
4	Professional Core Course	4CH04	Chemical Engg. Thermodynamics-II	3	-	-	3	3	3	80	20	100	40	---	---	---	---
5	Professional Core Course	4CH05	Chem. Engg. Operation –I (Mech. Operation)	3	-	-	3	3	3	80	20	100	40	---	---	---	---
6	Humanities & Social Science	4ES06	Environmental Studies	2	-	-	2	2	3	80	20	100	40	---	---	---	---
7	Engineering Science Course	4CH07	Applied Physical Chemistry-Lab	-	-	2	2	1	---	---	---	---	---	25	25	50	25
8	Professional Core Course	4CH08	Fluid Flow Operation-Lab	-	-	2	2	1	---	---	---	---	---	25	25	50	25
9	Professional Core Course	4CH09	Chem. Engg. Thermo.-II – Lab.	-	-	2	2	1	---	---	---	---	---	25	25	50	25
10	Professional Core Course	4CH10	Chem. Engg. Operation –I (Mech. Operation)- Lab	-	-	2	2	1	---	---	---	---	---	25	25	50	25
Total				**17**	**-**	**08**	**25**	**21**				600				200	
Grand Total												**600**				**200**	**800**

Note – **(i)** Environmental Science as per Ordinance no. 42/2005 **(ii)** For subject 4CH02 Machine Design & Drawing, Students are expected to submit minimum 5 drawing sheets.

L : Theory Lecture T : Tutorial P : Practical D : Drawing / Design	FOUR YEAR DEGREE COURSE IN BACHELOR OF TECHNOLOGY BRANCH: CHEMICAL ENGINEERING CREDIT GRADE SYSTEM SEMESTER PATTERN **SEMESTER : FIFTH**

Sr No.	Category	Subject Code	Subject	Teaching Scheme					Examination Scheme								
				L	T	P/D	Total Hour/ week	Credits	Duration of Papers (Hrs.)	Maximum Marks		Total	Min. Pass Marks	Max. Marks Practical		Total Marks	Maximum Passing Marks
										Theory Paper	College Assessment			External	Internal		
1	Professional Core Course	5 CH 01	Heat Transfer	3	1	-	4	4	3	80	20	100	40	---	---	---	---
2	Professional Core Course	5 CH 02	Chem. Engg. Process-I (Inorganic Chemical Technology)	3	1	-	4	4	3	80	20	100	40	---	---	---	---
3	Professional Core Course	5 CH 03	Material Science & Engineering	4	-	-	4	4	3	80	20	100	40	---	---	---	---
4	Professional Core Course	5 CH 04	Professional Elective-I	3	-	-	3	3	3	80	20	100	40	---	---	---	---
5	Professional Elective Course	5 CH 05	Open Elective- I	3	-	-	3	3	3	80	20	100	40	---	---	---	---
6	Professional Core Course	5 CH 06	Heat Transfer- Lab	-	-	2	2	1	---	---	---	---	---	25	25	50	25
7	Professional Core Course	5 CH 07	Material Science & Engineering Lab	-	-	2	2	1	---	---	---	---	---	25	25	50	25
Total				**16**	**2**	**4**	**22**	**20**				500				100	
											Grand Total	500				100	**600**

NOTES:

1. An Orientation Program / MOOC Courses of 15 hours duration on '**Indian Constitution'** to be offered to the students during the Fifth Semester.
2. Students have to select the **Open elective-**I from the other disciplines, offered by other departments or specialize expertise available in the institute.
3. List of **Open Elective-I** offered by Chemical Engineering Department**:**

A) Risk & Safety Management

4. List of **Professional Elective-I** :

a) Air Pollution Control

b) Economics and Management

Polymer Science and Technology Subject can be opt by students from chemical engineering and all other engineering descipline – **Offered by expertise from Polymer Technology**

****

L : Theory Lecture
T : Tutorial
P : Practical
D : Drawing / Design

FOUR YEAR DEGREE COURSE IN BACHELOR OF TECHNOLOGY
BRANCH: CHEMICAL ENGINEERING
CREDIT GRADE SYSTEM
SEMESTER PATTERN
SEMESTER : SIXTH

Sr. No.	Category	Subject Code	Subject	Teaching Scheme					Examination Scheme								
				L	T	P/ D	Total Hours /week	Credits	Duration of Papers (Hrs.)	Maximum Marks		Total	Min. Pass Marks	Max. Marks Practical		Total Marks	Maximum Passing Marks
										Theory Paper	College Assessment			External	Internal		
1	Professional Core Course	6 CH 01	Chemical Engg. Operation-II (Mass Transfer-I)	3	1	-	4	4	3	80	20	100	40	---	---	---	---
2	Professional Core Course	6 CH 02	Chemical Engg Process –II (Organic Chemical Technology)	3	-	-	3	3	3	80	20	100	40	---	---	---	---
3	Professional Core Course	6 CH 03	Computer Programming & Application	3	1	-	4	4	3	80	20	100	40	---	---	---	---
4	Professional Core Course	6 CH 04	Professional Elective- II	3	-	-	3	3	3	80	20	100	40	---	---	---	---
5	Professional Elective Course	6 CH 05	Open Elective - II	3	-	-	3	3	3	80	20	100	40	---	---	---	---
6	Professional Core Course	6 CH 06	Chemical Engg. Operation-II (Mass Transfer)- I Lab	-	-	2	2	1	---	---	---	---	---	25	25	50	25
7	Professional Core Course	6 CH 07	Computer Programming & Application-Lab	-	-	2	2	1	---	---	---	---	---	25	25	50	25
8	Project	6 CH 08	Minor Project/Skill Laboratory /Innov. Lab.	-	-	2	2	1	---	---	---	---	---	25	25	50	25
Total				**15**	**2**	**6**	**23**	**20**				500				150	
Grand Total												**500**				**150**	**650**

NOTES:

1. Orientation Program / MOOC Courses of 15 hours duration on '**Indian Traditional Knowledge'** to be offered to the students during the Sixth Semester

2. Students have to select the Open elective-II from the other disciplines, offered by other departments or specialize expertise available in the Institute.

3. **List of Open Electives-II** offered by Chemical Engineering Department :

A) Renewable Energy Sources

B) Composite Technology –

- Composite Technology – Subject can be opt by students from chemical engineering and all other engineering descipline- Which **Offered by expertise from Polymer Technology.**

4. **List of Professional Elective-II** :
(a) Process equipment Design and Drawing
(b) Fuel Technology

****

L : Theory Lecture
T : Tutorial
P : Practical
D : Drawing / Design

FOUR YEAR DEGREE COURSE IN BACHELOR OF TECHNOLOGY
BRANCH: CHEMICAL ENGINEERING
CREDIT GRADE SYSTEM
SEMESTER PATTERN
SEMESTER : SEVENTH

Sr. No.	Category	Subject Code	Subject	Teaching Scheme					Emamination Scheme								
				L	T	P/ D	Total Hours/ Week	Credits	Duration of Papers (Hrs.)	Maximum Marks		Total	Min. Pass Marks	Max.Marks Practical		Total Marks	Maximum Passing Marks
										Theory Paper	College Assesment			External	Internal		
1	Professional Core Course	7 CH 01	Chemical Engg Operation – III (Mass Transfer- II)	3	-	-	3	3	3	80	20	100	40	---	---	---	---
2	Professional Core Course	7 CH 02	Chem. Reaction Engineering – I	3	-	-	3	3	3	80	20	100	40	---	---	---	---
3	Professional Core Course	7 CH 03	Process Dynamics & Control	3	-	-	3	3	3	80	20	100	40	---	---	---	---
4	Professional Core Course	7 CH 04	Plant Design & Process Engg.	3	-	-	3	3	3	80	20	100	40	---	---	---	---
5	Professional Elective Course	7 CH 05	Professional Elective – 3	3	-	-	3	3	3	80	20	100	40	---	---	---	---
6	Professional Core Course	7 CH 06	Chemical Engg Operation – III (Mass Transfer- II)-Lab	-	-	2	2	1	---	---	---	---	---	25	25	50	25
7	Professional Core Course	7 CH 07	Chem. Reaction Engineering – I- Lab	-	-	2	2	1	---	---	---	---	---	25	25	50	25
8	Professional Core Course	7 CH 08	Process Dynamics & Control	-	-	2	2	1	---	---	---	---	---	25	25	50	25
9	Professional Elective	7 CH 09	Professional Elective-III Lab	-	-	2	2	1	---	---	---	---	---	25	25	50	25
10	Project	7 CH 10	Project & Seminar			8	8	4	---	---	---	---	---	-	50	50	25
			Total	**15**	**-**	**16**	**31**	**23**				**500**				**250**	
											Grand Total	**500**				**250**	**750**

NOTE 1: For Professional Elective -III

- The Elective course will be offered as per the availability of the faculty with College /institute & only if the number of students opting for such elective are higher.

7CH05: PROFESSIONAL ELECTIVE –III :

1. Industrial Waste Treatment
2. New Separation Techniques
3. Optimization of chemical Process
4. Smart Materials.

NOTE 2: For Industrial Training/ Internship :

During the course of study from III to VII semester each student is expected to undertake a minimum of two industrial visits and undertake a minimum of two weeks of industry/ field training/Internship. The students are expected to submit a report, which shall be evaluated by an internal assessment committee at the end of VII semester.

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L : Theory Lecture T : Tutorial P : Practical D : Drawing / Design	FOUR YEAR DEGREE COURSE IN BACHELOR OF TECHNOLOGY BRANCH: CHEMICAL ENGINEERING CREDIT GRADE SYSTEM SEMESTER PATTERN **SEMESTER : EIGHTH**

Sr. No.	Category	Subject Code	Subject	Teaching Scheme					Examination Scheme								
				L	T	P/D	Total Hours/ week	Credits	Duration of Papers (Hrs.)	Maximum Marks		Total	Min. Pass Marks	Max. Marks Practical		Total Marks	Maximum Passing Marks
										Theory Paper	College Assessment			External	Internal		
1	Professional Core Course	8 CH 01	Transport Phenomenon	3	-	-	3	3	3	80	20	100	40	---	---	---	---
2	Professional Core Course	8 CH 02	Chem. Reaction Engineering - II	3	-	-	3	3	3	80	20	100	40	---	---	---	---
3	Professional Core e Course	8 CH 03	System Modelling	3	-	-	3	3	3	80	20	100	40	---	---	---	---
4	Professional Elective Course-II	8 CH 04	Professional Elective – IV	3	-	-	3	3	3	80	20	100	40	---	---	---	---
5	Professional Elective Course	8 CH 05	Professional Elective – IV Lab.	-	-	2	2	1	---	---	---	---	---	25	25	50	25
6	Professional core Course	8CH06	Chem. Reaction Engineering-II lab	-	-	2	2	1	---	---	---	---	---	25	25	50	25
7	Professional Elective Course	8 CH 07	Project & Seminar	-	-	12	12	6	---	---	---	---	---	75	75	150	75
Total				**12**	**-**	**16**	**28**	**20**				**400**				**250**	
											Grand Total	400				250	**650**

Note: The Elective will be offered as per the availability of the faculty with the college /Institute & only if the number of student opting for such elective are minimum thirty.

8CH04 PROF. ELECTIVE –IV

1. Petrochemical Technology
2. Industrial Piping
3. Energy & Environment Enginneing

****

1.1.1 **The Institution ensures effective curriculum planning and delivery through a well-planned and documented process including Academic calendar and conduct of continuous internal Assessment**

4. Internal & External evaluation directions by Affiliating University

DIRECTION

No. 21/2020 Date :- 24/10/2020

Subject :- Examination leading to the Degree of B.E./ B.Text.E. /B.Tech. (Chem.Engg.) (Four Year Degree Course.. Semester Pattern) (C.B.C.S.) in the Faculty of Science & Technology, Direction 2020.

Whereas, Direction No. 29 of 2010 in respect of the Examination leading to the Degree of B.E./ B.Text.E. /B.Tech. (Chem.Engg.) (Four Year Degree Course .. Semester Pattern) (C.B.C.S.) in the Faculty of Engineering & Technology, Direction, 2010 of B.E. /B.Text. E.(Common to all branches) as per Credit Grade System in the Faculty of Engineering & Technology was in existence up to the session 2018-19 and abrogated stage wise vide Direction No. 26 /2019,

AND

Whereas, Direction Nos. 31/2011, 31/2012, 3/2013, 16/2014, 12/2016, 19/2016, 20/2016, 11/2017 and 37/2018 in respect of the Schemes of teaching & examination of Semesters III to VIII in the various branches of B.E. /B.Text.E. /B.Tech. (Chem. Tech.) as per Credit Grade System in the Faculty of Engineering & Technology are in existence,

AND

Whereas, Direction No. 26 of 2019 in respect of the Examination leading to the Degree of B.E./ B.Text.E. /B.Tech.(Chem.Engg.), B.Tech.(Chem. Tech.) (Polymer) (Plastic) Tech. (Four Year Degree Course..Semester Pattern) (C.B.C.S.) in the Faculty of Science & Technology, Direction, 2020 is in existence,

AND

Whereas, the Hon'ble Vice-Chancellor had constituted a Committee of all the Chairpersons of the Board of Studies of Engineering & Technology under the Chairmanship of the Dean, Faculty of Science & Technology for preparing of the Schemes of teaching & examination of Under Graduated Courses of Semester III to VIII of B.E. /B.Text.E. / B.Tech. (Chem.Engg.) / B.Tech. (Chem.Tech.) as per the guidelines of A.I.C.T.E. Model Curriculum to be implemented from the session 2020-21 & onwards in phase wise manner,

AND

Whereas, the Committee in its series of meetings dtd. 6.6.2020, 22.6.2020 & 23.6.2020 has prepared, finalized and recommended the Schemes of teaching & examination of the branches Civil Engg., Mechanical Engg., Electronics & Telecommunication Engg., Computer Science & Engg. / Computer Engg., Electrical Engg., Electrical Engg. (Electronics & Power), Electrical & Electronics Engg., Information Technology, Textile Engg., Chemical Engg., (C.B.C.S.) of Semester III to VIII as per guidelines of AICTE Model Curriculum to the office to be implemented from the session 2020-21 & onwards in phase wise manner,

AND

Whereas, the Hon'ble Vice-Chancellor had accepted and accorded approval to the schemes of teaching & examination of Semester III to VIII of B.E. /B.Text.E. /B.Tech. (Chem.Engg.) on behalf of Faculty of Science & Technology and Academic Council on 24.7.2020 to be implemented from the session 2020-21 & onwards in phase wise manner,

AND

Whereas, the above Schemes of teaching & examinations of Semesters Semester III to VIII of B.E. /B.Text.E./B.Tech.(Chem.Engg.) in the Faculty of Science & Technology are required to be regulated by the Ordinance /Regulation,

AND

Whereas, making the Ordinance /Regulation is a time consuming process,

Now, therefore, I, Dr. M.G.Chandekar, Vice-Chancellor, Sant Gadge Baba Amravati University, in exercise of powers conferred upon me under sub-section (8) of Section 12 of the Maharashtra Public Universities Act, 2016, do hereby direct as under :-

(1) This Direction shall be called "Examination leading to the Degree of B.E./ B.Text.E. /B.Tech. (Chem.Engg.) (Four Year Degree Course..Semester Pattern) (C.B.C.S.) in the Faculty of Science & Technology, Direction, 2020".

(2) This Direction shall come into force from the date of its issuance.

(3) Subject to the conditions prescribed by the Government from time to time, for admission to First Year B.E./B.Text.E. / B.Tech. (Chem. Engg.) / B.Tech. (Chem. Tech.) Polymer (Plastic) Tech. courses the candidate shall be considered eligible :

Passing 12th Standard examination of the Maharashtra State Board of Secondary and Higher Secondary Education, with subjects :

1. English (Higher or Lower)
2. Modern Indian Language (Higher or Lower)
3. Mathematics and Statistics.

4. Chemistry.
5. Physics.
6. Any other optional subject from out of the list prescribed by the said Secondary and Higher Secondary Education Board.

OR

i) English (Higher or lower)
ii) Mathematics and Statistics.
iii) Chemistry
iv) Physics
v) Vocational subject (Defined by the said Board as a Technical Subject)

OR

An Examination recognised by the Sant Gadge Baba Amravati University as an equivalent to the above.

(4) Subject to the conditions prescribed by the Govt. from time to time for direct admission to the second Year B.E. / B.Text.E. / B.Tech. (Chem. Engg.) / B.Tech. (Chem. Tech.) Polymer (Plastic) Tech. the candidates shall be considered eligible :-

Passing Diploma in relevant branch in First Division, awarded by the Board of Technical Examination of Maharashtra State, Mumbai.

OR

Any Diploma equivalent to the corresponding Diploma of the Board of Technical Examination of Maharashtra State, Mumbai.

(5) (a) The Degree of Bachelor of Engineering shall be awarded to examinee who in accordance with the provisions of this Direction qualifies for the award in any of the following branches.

i. Civil Engineering
ii. Mechanical Engineering
iii. Electrical Engineering (Electronics & Power)
iv. Electrical Engineering
vi. Electrical and Electronics Engineering.
vii. Electronics and Telecommunication Engineering
viii. Computer Science & Engineering
ix. Information Technology
x. Computer Engineering
xi. Chemical Engineering
xii. Textile Engineering

(a) The Degree of Bachelor of Textile Engineering shall be awarded to examinee, who qualifies in accordance with the provisions of this Direction.
(b) The Degree of Bachelor of Technology (Chemical Engineering) shall be awarded to examinee who qualifies in accordance with the provisions of this Direction.
(c) The Degree of Bachelor of Technology (Chemical Technology) Polymer (Plastic) Tech. shall be awarded to examinee who qualifies in accordance with the provisions of this Direction.

(6) (i) There shall be eight semester examinations leading to the Degree of B.E./B.Text.E./B.Tech. (Chem. Engg.) /B.Tech. (Chem. Tech.) Polymer (Plastic) Tech. (First, Second, Third, Fourth, Fifth, Sixth, Seventh & Eight Semester)
(ii) The first & Second Semester Examinations shall be common for all the branches.
(iii) The procedure for bifurcation of the students in Group - A & Group - B shall be as given in **Appendix -B**.

(7) The period of Academic Session shall be such as may be notified by the University.

(8) The main examination of first, third, fifth and seventh semester shall be held by the University in winter & supplementary examination in summer every year. And main examination of second, fourth, sixth & eighth semester shall be held in summer & the supplementary examination in winter every year.

(9) The Internal Assessment marks for theory should be based on Class Test and Attendance as follows:-

(a) Class Test Marks will be based upon two Class Tests.	-	15
(b) Attendance	-	Mark/s
75% to 80%	-	1
81% to 85%	-	2
86% to 90%	-	3
91% to 95%	-	4
96% to 100%	-	5

Wherever, if internal assessment marks are ‘ten (10)’ then it should be converted out of “20”.

(10) Subject to his/her compliance with the provisions of this Direction & other Ordinances pertaining to Examination in force from time to time, the applicant for admission, at the end of the course of study of a particular semester/session, to an Examination specified in column (1) of the table I below, shall be eligible to appear if,

i) he/she satisfies with the conditions in the table and the provisions there under.
ii) he/she complies with the provisions of the ordinance pertaining to the Examination in general from time to time.
iii) he/she has prosecuted a regular course of study in a college affiliated to the University.

iv) he/she has in the opinion of the Principal shown satisfactory progress in his/her studies.

TABLE I

Name of Exam B.E./B.Text.E./ B.Tech. (Chem. Engg.)/B.Tech. (Chem.Tech.) Polymer (Plastic)Tech.	The student should have passed Exam. of	The Student should have satisfactorily completed the following semester	The student should have passed the following examination
1.	2.	3.	
First Semester Group A/Group B	XII standard Examination or equivalent	....	....
Second Semester Group A/Group B	....	I Semester Group A/Group B	.....
Third Semester	....	II Semester Group A/Group B	2/3rd heads of I & II Sem. combined together
Fourth Semester	.....	III Semester	.....
Fifth Semester	I & II Sem.	IV Semester	2/3rd heads of III & IV Sem. combined together
Sixth Semester	....	V Semester	.....
Seventh Semester	III & IV Sem. combined together	VI Semester	2/3rd heads of V & VI Sem.
Eighth Semester	.....	VII Semester	.....

(11) An examinee who has passed 2/3 rd heads of passing shall be allowed to keep term in the next higher class.
Explanation:
(i) While calculating 2/3 rd heads of passing, fraction if any shall be ignored
(ii) For considering the heads of passing, every theory and every practical shall be considered as separate head of passing.

(12) The schemes of teaching & examinations shall be as provided under "**Appendix-A**" appended with this Direction.

(13) The fees for each B.E./B.Text.E./B.Tech. (Chem. Engg.)/B.Tech. (Chem. Tech.) Polymer (Plastic) Tech. Examinations (Theory & Practical) shall be as prescribed by University from time to time.

(14) The computation of Semester Grade Point Average (SGPA) and Cumulative Grade Point Average (CGPA) of an examinee shall be done as given below :-

The marks will be given in all examinations which will include college assessment marks and the total marks for each Theory / Practical shall be converted into Grades as per **Table II**.

SGPA shall be calculated based on Grade Points corresponding to Grade as given in Table II and the Credits allotted to respective Theory / Practical shown in the scheme for respective semester.

SGPA shall be computed for every semester and CGPA shall be computed only in VIII semester. The CGPA of VIII semester shall be calculated based on SGPA of VII and SGPA of VIII semester as per following computation :-

$$\text{SGPA} = \frac{C_1 \times G_1 + C_2 \times G_2 + \ldots\ldots + C_n G_n}{C_1 + C_2 + \ldots\ldots\ldots + C_n}$$

Where, C_1 = Credit of individual Theory / Practical
G_1 = Corresponding Grade Point obtained in the respective Theory / Practical

$$\text{CGPA} = \frac{(\text{SGPA})_{VII} \times (\text{Cr})_{VII} + (\text{SGPA})_{VIII} \times (\text{Cr})_{VIII}}{(\text{Cr})_{VII} + (\text{Cr})_{VIII}}$$

Where,

$(\text{SGPA})_{VII}$	=	SGPA of VII Semester
$(\text{Cr})_{VII}$	=	Total Credits for VII Semester
$(\text{SGPA})_{VIII}$	=	SGPA of VIII Semester
$(\text{Cr})_{VIII}$	=	Total Credits for VIII Semester

PRACTICAL

Grade	Percentage of Marks	Grade Points
AA	85 ≤ Marks ≤ 100	10
AB	80 ≤ Marks < 85	9
BB	75 ≤ Marks < 80	8
BC	70 ≤ Marks < 75	7
CC	65 ≤ Marks < 70	6
CD	60 ≤ Marks < 65	5
DD	50 ≤ Marks < 60	4
FF	00 ≤ Marks < 50	0
ZZ	Absent in Examination	—

(15) (i) The scope of the subjects shall be as indicated in the syllabi.
(ii) The medium of instruction and examination shall be English.

(16) The Schemes of teaching & examination of Semester I & II (Group A & B) of B.E. /B.Text. E./B.Tech. (Chem.Engg.)/ B.Tech. (Chem. Tech.) (Polymer) (Plastic) Tech. had been already implemented from the session 2019-2020 which was notified vide Direction No. 26/2019.

(17) As per A.I.C.T.E. Model Curriculum, an Induction Program of three (3) weeks duration is mandatory to the students at the start of the first semester.

(18) The Schemes of teaching & examination of Semester III to VIII of B.E./ B.Text.E./ B.Tech. (Chem.Engg.) (C.B.C.S.) of the branches Civil Engg., Mechanical Engg., Electronics & Telecommunication Engg., Computer Science & Engg., Computer Engg., Electrical Engg., Electrical Engg. (Electronics & Power), Electrical & Electronics Engg., Information Technology, Textile Engg., Chemical Engg., (C.B.C.S.) as per A.I.C.T.E. Model Curriculum shall be implemented in phase wise manner as under :

(i) For Semester III & IV from the session - 2020-2021
(ii) For Semester V & VI from the session - 2021-2022
(iii) For Semester VII & VIII from the session - 2022-2023

(19) The Schemes of teaching & examination of Semester I & II of B.E. / B.Text.E./ B.Tech. (Chemical Engg.) (common to all branches) and Semester III to VIII of the branches Civil Engg., Mechanical Engg., Electronics & Telecommunication Engg., Computer Science & Engg., Computer Engg., Electrical Engg., Electrical Engg. (Electronics & Power), Electrical & Electronics Engg., Information Technology, Textile Engg., Chemical Engg., (C.B.C.S.) as per A.I.C.T.E. Model Curriculum shall be as per Appendices A,B,C,D,E,F,G,H,I,J,K and L appended with this Direction.

(20) (i) The Semester wise chart regarding the workload and Credits as per A.I.C.T.E. Model Curriculum guidelines for Engineering & Technology Courses for the Schemes of teaching & examination of Sem. III to VIII is as under :

CHART

Sem.	Theory	Pract.	Theory credits	Pract. Credits	Semester Credits	Hours/ week	Remarks
I	4	4	15	5	20	25	Started from session 2019-20
II	4	4	15	5	20	25	
III	5	4	16	4	20	26	ES 2T, 0 credit
IV	5	4	18	4	22	26	ES 2T, 2 credits
V	5	4	16	4	20	24	PE-1,OE-1
VI	5	4	16	4	20	24	PE-1,OE-1
VII	5	3	16	3+4	23	30	PE-2 or 3, Project seminar - 8 hrs, 4 credits
VIII	4	2	12	2+6	20	28	PE-1 or 2, Project seminar 12hrs, 6 credits
Total	**37**	**29**	**124**	**41**	**165**		

(ii) The workload for the subject Environment Studies for Semester III & IV (3ES06 & 4ES06) which is common for all branches in all the Faculties as per Ordinance No. 42/2005 is as : 2 theory in III semester with no credits, 2 theory in IV semester with 2 credits and examination at the end of IV semester at college level having distribution as : 80 (Max. marks for Theory) + 20 (Internal) = 100 (Total marks) – 40 (Minimum marks for passing)

(iii) Open Electives (OE): Open Elective to be opted from the courses offered by other disciplines of Engineering & Technology of the university / Massive Open learning Courses (MOOC) such as SWAYAM pertaining to the profession.

(iv) Students completing foreign language course or completing minimum 4 weeks internship (Full time in Vacations) or participating in sports at National / International level shall be exempted from O.E. in the same / adjacent semester.

(v) An Orientation Program of 15 hours duration /MOOC to be offered to the students during (a)VthSemester : Indian Constitution (b) VIth Semester: Indian Traditional Knowledge.

(21) The Provisions of Ordinance No. 18 of 2001 in respect of an Ordinance to provide grace marks for passing in a Head of passing and improvement of division (Higher Class) and getting distinction in the subject and condonation of deficiency of marks in a subject in all the Faculties prescribed by the Direction No. 15 of 2017 shall be applicable to each examination under this Direction.

(22) An examinee who does not pass; or who fails to present himself/herself for the examination shall be eligible for re-admission to the same examination/semester, on payment of fresh fees and such other fees as may be prescribed from time to time.

(23) A candidate who could not complete a semester satisfactorily or who has failed will be eligible for readmission to the same semester.
However, re-admission to semester should be allowed only when a regular session is running for the particular semester.

(24) One who has passed the Final B.E./B.Text.E./B.Tech. (Chem. Engg.)/B.Tech. (Chem. Tech.) Polymer (Plastic) Tech. examination of the University in one branch and who desires to take B.E./B.Text.E./B.Tech.(Chem. Engg.)/ B.Tech. (Chem. Tech.) Polymer (Plastic) Tech. Degree in another branch shall be admitted to the third Semester of that branch and shall be governed by this Direction for all other purposes.

(25) After examinations the Board of Examination & Evaluation shall publish the result of the examinees as early as possible and the branch wise merit list shall be notified as per Ordinance No.6.

(26) Notwithstanding anything to the contrary in this Direction, no one shall be admitted to any examination under this Direction, if he/she has already passed the said examinations or an equivalent examinations of any statutory University.

(27) (i) The examinees who have passed in all the subjects prescribed for all the examinations of the particular branch shall be eligible for award of the Degree of Bachelor of Engineering / Bachelor of Technology (Chemical Technology) Polymer (Plastic) in the branch concerned, Bachelor of Textile Engineering and Bachelor of Technology (Chemical Engineering).

(ii) The Degree certificate in the prescribed form shall be signed by the Vice-Chancellor.

(28) The Guidelines of the A.I.C.T.E. New Delhi and D.T.E., Govt. of Maharashtra, Mumbai shall be applicable from time to time after having noted / approved by the Competent Authority.

(29) The existing Direction No. 26/2019 shall stand abrogated stage wise and only applicable to the students who have already sought their admissions as per its provisions and shall abrogated after exhausting the chances given to the failure students of Semester I /II (Group A & B) of B.E. /B.Text. E./B.Tech. (Chem.Engg.) of the University.

(**30**) The provisions in existing Direction Nos. 31/2011, 31/2012, 3/2013, 16/2014, 12/2016, 11/2017 and 37/2018 shall stand only be applicable to the students of Semester III to VIII of the branches Civil Engg., Mechanical Engg., Production Engg., Electronics & Telecommunication Engg., Electronics Engg., Instrumentation Engg., Computer Science & Engg., Computer Engg., Electrical Engg., Electrical Engg. (Electronics & Power), Electrical Engg. (Electrical & Power), Electrical & Electronics Engg., Information Technology, Textile Technology, Chemical Engg., Chemical Technology (Polymer) (Plastic) and Biomedical Engg. who have already sought their admissions as per its provisions and shall stand abrogated after exhausting the chances given to the failure students of Old Course by the University.

Sd/-
Date :- 24/10/2020 (Dr.M. G.Chandekar)
Vice Chancellor

5. Unit Test Time Table NOTICES/DIRECTIONS

Anuradha Engineering College, Chikhli
Department of Information Technology
Session: 2022-23 (Summer 2023)
Unit Test-II

Date: 24-05-2023

Notice:

All the staff members are hereby requested to note down the schedule of Unit Test – II examination (4th Sem) follow the guidelines given below.

1.	Submission of Unit Test model question paper (of 30 marks) in soft copy to the departmental Co-ordinator. Format of Question Paper – Q. 1 a, b **OR** Q. 2 a, b and Q. 3 a, b **OR** Q. 4 a, b	On or before 26-05-2023
2.	Examination Schedule	29-05-2023 To 31-05-2023
3.	Period for valuation of answer sheets & Circulation of valued answer sheet among students. (40% passing)	Within 01 days after conduction of unit test of concern subject
4.	Submission of control sheet to the departmental Unit Test Co-ordinator.	Within 03 days after conduction of unit test of concern subject.
5.	Declaration of result. (Departmental Co-ordinator)	02-06-2023

Sawale

Ms. S. T. Sawale
Unit Test Co-ordinator

Dr. A. S. Kapse
Head of Department
Information Technology
A. E. C. Chikhli Dist. Buldana

ANURADHA ENGINEERING COLLEGE, CHIKHLI

Department of Information Technology

Session: 2022-23 (Summer-2023)

Unit Test Time Table - II

Date: 24/05/2023

Date	Time	Semester	Subject
29-05-2023 Monday	11:00 am – 12:30 pm	4th	CO&A (4IT01)
	03:00 pm – 04:30 pm	4th	DCN (4IT02)
30-05-2023 Tuesday	11:00 am – 12:30 pm	4th	OS (4IT03)
	03:00 pm – 04:30 pm	4th	Data. Stru. (4IT04)
31-05-2023 Wednesday	01:30 am – 03:00 pm	4th	SSEE (4IT05)
	04:00 pm – 05:30 pm	4th	EVS (4ES06)

Sawale

Ms. S. T. Sawale
Unit Test Co-ordinator

Dr. A.S. Kapse
Head of Department
Information Technology
A. E. C. Chikhli. Dist. Buldana

ANURADHA ENGINEERING COLLEGE, CHIKHLI

Department of Information Technology
Session: 2022-23 (Summer-2023)
Unit Test Time Table

Date: 20/04/2023

Date	Time	Semester	Subject
27-04-2023 Thursday	11:00 am – 12:30 pm	4th	CO&A (4IT01)
		6th	CD (6IT01)
		8th	OOA&D (8IT01)
	03:00 pm – 04:30 pm	4th	DCN (4IT02)
		6th	D&AA (6IT02)
		8th	PE&M (8IT02)
28-04-2023 Friday	11:00 am – 12:30 pm	4th	OS (4IT03)
		6th	AI (6IT03)
		8th	PM&E (8IT03)
	03:00 pm – 04:30 pm	4th	Data. Stru. (4IT04)
		6th	Professional Elective – II (6IT04) Cryptography & Network Security
		8th	Professional Elective – V (8IT04) Human Computer Interaction
29-03-2023 Wednesday	11:00 am – 12:30 pm	4th	SSEE (4IT05)
		6th	Open Elective-II (EXTC) Wireless Communication
	03:00 pm – 04:30 pm	4th	EVS (4ES06)

Sawale 20/4/2023

Ms. S. T. Sawale
Unit Test Co-ordinator

Dr. A.S. Kapse
Head of Department
Information Technology
A. E. C. Chikhli. Dist. Buldana

Anuradha Engineering College, Chikhli

Department of Information Technology

Session: 2022-23 (Summer 2023)

Unit Test

Date: 20-04-2023

Notice:

All the staff members are hereby requested to note down the schedule of Unit Test – II examination (6th Sem and 8th Sem Only) and Unit Test-I (4th Sem) follow the guidelines given below.

1.	Submission of Unit Test – I model question paper (of 30 marks) in soft copy to the departmental Co-ordinator. Format of Question Paper – Q. 1 a, b **OR** Q. 2 a, b and Q. 3 a, b **OR** Q. 4 a, b	On or before 24-04-2023
2.	Examination Schedule	27-04-2023 To 29-04-2023
3.	Period for valuation of answer sheets & Circulation of valued answer sheet among students. (40% passing)	Within 01 days after conduction of unit test of concern subject
4.	Submission of control sheet to the departmental Unit Test Co-ordinator.	Within 03 days after conduction of unit test of concern subject.
5.	Declaration of result. (Departmental Co-ordinator)	04-05-2023

Sawale

Ms. S. T. Sawale
Unit Test Co-ordinator

Dr. A. S. Kapse
Head of Department
Information Technology
A. E. C. Chikhli. Dist. Buldana

ANURADHA ENGINEERING COLLEGE, CHIKHLI

Department of Information Technology

Session: 2022-23 (Summer-2023)

Unit Test – I Time Table

Date: 20/03/2023

Date	Time	Semester	Subject
27-03-2023 Monday	11:00 am – 12:30 pm	6th	CD (6IT01)
		8th	OOA&D (8IT01)
	03:00 pm – 04:30 pm	6th	D&AA (6IT02)
		8th	PE&M (8IT02)
28-03-2023 Tuesday	11:00 am – 12:30 pm	6th	AI (6IT03)
		8th	PM&E (8IT03)
	03:00 pm – 04:30 pm	6th	Professional Elective – II (6IT04) Cryptography & Network Security
		8th	Professional Elective – V (8IT04) Human Computer Interaction
29-03-2023 Wednesday	11:00 am – 12:30 pm	6th	Open Elective-II (EXTC) Wireless Communication

Ms. S. T. Sawale
Unit Test Co-ordinator

Dr. A.S. Kapse
Head of Department
Information Technology
A. E. C. Chikhli. Dist. Buldana

Anuradha Engineering College, Chikhli
Department of Information Technology
Session: 2022-23 (Summer 2023)
Unit Test-I

Date: 20-03-2023

Notice:

All the staff members are hereby requested to note down the schedule of Unit Test – I examination (6th Sem and 8th Sem Only) and follow the guidelines given below.

1.	Submission of Unit Test – I model question paper (of 30 marks) in soft copy to the departmental Co-ordinator. Format of Question Paper – Q. 1 a, b **OR** Q. 2 a, b and Q. 3 a, b **OR** Q. 4 a, b	On or before 23-03-2023
2.	Examination Schedule	27-03-2023 To 29-03-2023
3.	Period for valuation of answer sheets & Circulation of valued answer sheet among students. (40% passing)	Within 01 days after conduction of unit test of concern subject
4.	Submission of control sheet to the departmental Unit Test Co-ordinator.	Within 03 days after conduction of unit test of concern subject.
5.	Declaration of result. (Departmental Co-ordinator)	05-04-2023

Sawale

Ms. S. T. Sawale
Unit Test Co-ordinator

Dr. A. S. Kapse
Head of Department
Information Technology
A. E. C. Chikhli Dist. Buldana

ANURADHA ENGINEERING COLLEGE, CHIKHLI

Department of Information Technology

Session: 2022-23

TIME TABLE

UNIT TEST – II

Date: 07 /01/2023

Date	Time	Semester	Subject
11-01-2023 Wednesday	11:00 am – 12:30 pm	3rd	M-III (3IT01)
	03:00 pm – 04:30 pm	3rd	DS&GT (3IT02)
12-01-2023 Thursday	11:00 am – 12:30 pm	3rd	OOP (3IT03)
	03:00 pm – 04:30 pm	3rd	ALP (3IT04)
13-01-2023 Friday	11:00 am – 12:30 pm	3rd	A&DE (3IT05)

Sawale 7/1/2023

Ms. S. T. Sawale
Unit Test Co-ordinator

A.S.K

Dr. A.S. Kapse
Head of Department
Information Technology
A. E. C. Chikhli, Dist. Buldana

Anuradha Engineering College, Chikhli
Department of Information Technology
Even Semester 2022-23
Unit Test-II (3rd Sem.)

Date: 07-01-2023

Notice:

All the staff members are hereby requested to note down the schedule of Unit Test – II examination and follow the guidelines given below.

Sr. No.	Particulars	Schedule
1.	Submission of Unit Test – II model question paper (30 marks =15+15) in soft copy to the departmental Co-ordinator. Format of Question Paper – Q. 1 a, b OR Q. 2 a, b and Q. 3 a, b OR Q. 4 a, b	On or before 09-01-2023
2.	Examination Conduction	11-01-2023 To 13-01-2023
3.	Period for valuation of answer sheets & Circulation of valued answer sheet among students. (40% passing)	Within 03 days after conduction of unit test of concern subject
4.	Submission of control sheet to the departmental Unit Test Co-ordinator.	Within 03 days after conduction of unit test of concern subject.
5.	Declaration of result.	16-01-2023

Sawale 7/1/2023
Ms. S. T. Sawale
Unit Test Co-ordinator

Dr. A.S. Kapse
Head of Department
Information Technology
A. E. C. Chikhli, Dist. Buldana

1. PTT -
2. STS -
3. PSI -
4. NBM -

ANURADHA ENGINEERING COLLEGE, CHIKHLI

Department of Information Technology

Session: 2022-23

TIME TABLE FOR UNIT TEST – II

Date: 18/11/2022

Date	Time	Semester	Subject
23-11-2022 Wednesday	11:00 am – 12:30 pm	5th	DBMS (5IT01)
		7th	MC (7IT01)
	03:00 pm – 04:30 pm	5th	TOC (5IT02)
		7th	ES (7IT02)
24-11-2022 Thursday	11:00 am – 12:30 pm	5th	SE (5IT03)
		7th	CC (7IT03)
	03:00 pm – 04:30 pm	5th	ISS- PE I (5IT04)
		7th	DW&M – PE III (7IT04)
25-11-2022 Friday	11:00 am – 12:30 pm	5th	DS- OE I (5ETC05)
	11:00 am – 12:30 pm	7th	BCF- PE IV (7IT05)

Sawale

Ms. S. T. Sawale
Unit Test Co-ordinator

Dr. A.S. Kapse
Head of Department
Information Technology
A.E.C. Chikhli, Dist. Buldana

Anuradha Engineering College, Chikhli
Department of Information Technology
Even Semester 2022-23
Unit Test-II

Date: 18-11-2022

Notice:

All the staff members are hereby requested to note down the schedule of Unit Test – II examination and follow the guidelines given below.

Sr. No.	Particulars	Schedule
1.	Submission of Unit Test – II model question paper (30 marks =15+15) in soft copy to the departmental Co-ordinator. Format of Question Paper – Q. 1 a, b OR Q. 2 a, b and Q. 3 a, b OR Q. 4 a, b	On or before 22-11-2022
2.	Examination Conduction	23-11-2022 To 25-11-2022
3.	Period for valuation of answer sheets & Circulation of valued answer sheet among students. (40% passing)	Within 03 days after conduction of unit test of concern subject
4.	Submission of control sheet to the departmental Unit Test Co-ordinator.	Within 03 days after conduction of unit test of concern subject.
5.	Declaration of result.	28-11-2022

Sawale

Ms. S. T. Sawale
Unit Test Co-ordinator

Dr. A.S. Kapse
Head of Department
Information Technology
A. E. C. Chikhli, Dist. Buldana

1. PTT -
2. STS -
3. PSI -
4. NBM -

ANURADHA ENGINEERING COLLEGE, CHIKHLI

Department of Information Technology

Session: 2022-23

TIME TABLE FOR UNIT TEST – I

Date: 03/10/2022

Date	Time	Semester	Subject
13-10-2022 Thursday	11:00 am – 12:30 pm	3rd	M-III
		5th	DBMS
		7th	CC
	03:00 pm – 04:30 pm	3rd	DS&GT
		5th	TOC
		7th	MC
14-10-2022 Friday	11:00 am – 12:30 pm	3rd	OOP
		5th	SE
		7th	ES
	03:00 pm – 04:30 pm	3rd	ALP
		5th	Professional Elective - I Information Security System
		7th	Professional Elective - III Data Warehousing & Mining
15-10-2022 Saturday	11:00 am – 12:30 pm	3rd	A&DE
		5th	Open Elective-I Data Structure (EXTC)
		7th	Professional Elective - IV Block Chain Fundamental

Sawale 3/10/22

Ms. S. T. Sawale
Unit Test Co-ordinator

3/10/2022

Dr. A.S. Kapse
Head of Department
Information Technology
A. E. C. Chikhli Dist. Buldana

Anuradha Engineering College, Chikhli
Department of Information Technology
Session: 2022-23 (Winter 2022)
Unit Test-I

Date: 03-10-2022

Notice:

All the staff members are hereby requested to note down the schedule of Unit Test – I examination and follow the guidelines given below.

1.	Submission of Unit Test – I model question paper (of 30 marks) in soft copy to the departmental Co-ordinator. Format of Question Paper – Q. 1 a, b **OR** Q. 2 a, b and Q. 3 a, b **OR** Q. 4 a, b	On or before 10-10-2022
2.	Examination Schedule	13-10-2022 To 15-10-2022
3.	Period for valuation of answer sheets & Circulation of valued answer sheet among students. (40% passing)	Within 01 days after conduction of unit test of concern subject
4.	Submission of control sheet to the departmental Unit Test Co-ordinator.	Within 03 days after conduction of unit test of concern subject.
5.	Declaration of result. (Departmental Co-ordinator)	20-10-2022

Sawale
Ms. S. T. Sawale
Unit Test Co-ordinator

3/10/22
Dr. A. S. Kapse
Head of Department
Information Technology
A. E. C. Chikhli, Dist. Buldana

1. PTT -
2. STS - Sawale
3. NNK - 10/4
4. NBM -
5. PSI -
6. PSG -
7. DGV -
8. PRK - 10/10/22
9. APB -
10. [redacted] -

ANURADHA ENGINEERING COLLEGE, CHIKHLI

Department of Information Technology

Session: 2022-23

TIME TABLE FOR UNIT TEST – I

Date: 03/10/2022

Date	Time	Semester	Subject
13-10-2022 Thursday	11:00 am – 12:30 pm	3rd	M-III
		5th	DBMS
		7th	CC
	03:00 pm – 04:30 pm	3rd	DS&GT
		5th	TOC
		7th	MC
14-10-2022 Friday	11:00 am – 12:30 pm	3rd	OOP
		5th	SE
		7th	ES
	03:00 pm – 04:30 pm	3rd	ALP
		5th	Professional Elective - I ISS
		7th	PE-III ML Data Warehouse & Data Mining
15-10-2022 Saturday	11:00 am – 12:30 pm	3rd	A&DE
		5th	Open Elective-I Data Structure (EXTC)
		7th	PE-IV BCF

Sawale

Ms. S. T. Sawale
Unit Test Co-ordinator

A.S.K. 31/10/22

Dr. A.S. Kapse
Head of Department
Information Technology
A. E. C. Chikhli. Dist. Buldana

7. Teaching Plan

Anuradha Engineering college , Chikhli

Department of Mechanical Engg.

Teaching Plan

Semester :-3rd **Subject :- ETD**

Subject Teacher:- **Subject Code :- 3ME04**

Unit	Lecture No.	Topic to be Tought
1	1	Introduction to basic concept of thermodynamics, Microscopic and microscopic approaches,
	2	Properties of system, state and equilibrium, processes and cycle, temperature and Zeroth law of thermodynamics,
	3	Quasi-static process, forms of energy and conversion
	4	Gas law and ideal equation of states
	5	Difference between gases and vapors
	6	Equation of state, gas constant and universal gas constant.
	7	Problems on Unit-1
	8	Problems on Unit-1
	9	Problems on Unit-1
	10	Problems on Unit-1
2	11	Work and Heat: definition of work, thermodynamic work, displacement work, and other forms of work,
	12	Definition of heat, heat and work transfer as path function,
	13	Comparison of work and heat,
	14	Work done during various processes, pv diagram.
	15	First law of thermodynamics: energy of a system,
	16	Classification of energy, law of conversion of energy,
	17	Law applied to closed system undergoing cycle,
	18	Joules experiment, energy a property of system
	19	internal energy as a property of system, enthalpy,
	20	Specific heat at constant volume and pressure,
	21	Change in internal energy and heat transfer during various non-flow processes.
	22	Problems on Unit-2
3	21	Steady state and steady flow processes,
	22	Mass balance and energy balance in steady flow process,
	23	Steady flow energy equation and
	24	Its application to nozzle and diffusers,
	25	Turbine and compressor pumps, heat exchangers,
	26	Throttle valve etc. work done and heat transfer during steady flow processes.
	27	Review and Problems on Unit-3
	28	Problems on Unit-3
	29	Problems on Unit-3
	30	Problems on Unit-3
4	31	**Second law of thermodynamics:**
	32	Limitation of first law, thermal reservoir,
	33	Heat engine, refrigerator

	34	Heat pump,
	35	Kelvin –plank statements, their equivalence,
	36	Reversible and irreversible processes,
	37	Carnot cycle,
	38	Two propositions regarding the efficiency of Carnot cycles.
	39	The thermodynamics temperature scale. Reverse Carnot cycle.
	40	COP of heat pump and refrigerator. Inequality of Clausius.
	41	Problems on Unit-4
	42	Problems on Unit-4
5	43	Entropy as a property of system,
	44	Entropy change for ideal gases,
	45	Entropy change for system during irreversible process, lost work. Principle of increase of entropy.
	46	Availability and irreversibility: available energy refereed to cycle,
	47	Decrease in available energy, with heat transfer through finite temperature differences.
	48	The Helmhltz and Gibbs functions. Availability, irreversibility and effectiveness.
	49	Problems on Unit-5
	50	Problems on Unit-5
6	51	Air standard cycle: Otto, diesel,
	52	dual/semi-diesel,
	53	Sterling and joule cycles etc.
	54	Their efficiencies and mean effective pressure.
	55	Their efficiencies and mean effective pressure.
	56	Vapour cycles: Rankine and modified Rankine cycle.
	57	Comparison of Rankine and Carnot cycle.
	58	Representation of cycles on P-V, T-S and H-S diagram
	59	Representation of cycles on P-V, T-S and H-S diagram (no numerical included)
	60	Representation of cycles on P-V, T-S and H-S diagram (no numerical included)

Books Recommended

Text Books

1. Engineering Thermodynamic - by P.K.Nag.
2. Thermodynamics Volume: I & II; R. Yadav;

Reference Books

1. Basic Engineering Thermodynamics - by Reyner Joel
2. Thermodynamics - by C.P. Arora.
3. Fundamentals of Classical Thermodynamics - by G.J.Vanwylen.
4. Engineering Thermodynamics; P. Chattopadhyay; Oxford
5. Engineering Thermodynamics; Gordon Rogers, Yon Mayhew; Pearson

Prof.A.S.Patil

Subject in charge

Head of Dept.
Mechanical Engg. Dept.
Anuradha Engg. College, Chikhli

8. **Syllabus Completion Report**

Date 22/12/22

Anuradha Engineering College, Chikhli.
Department of Mechanical Engineering
Session-I (2022-23)
Syllabus Completion Report

Semester	Sr. No.	Name of Staff	Subject	No. of Lectured Conducted	Syllabus Covered
3rd Sem	1	Prof. V.R.Tekade	M-III	52	06 Units
	2	Prof. V.N.Jeughale	MOM	48	06 Units
	3	Prof. M.S.Sonune	ETD	46	06 Units
	4	Prof. A.V.Deshmukh	MP	52	06 Units
	5	Prof. M.R.Kale	FM	48	06 Units
5th Sem	1	Prof. A.M.Jumle	MS	46	06 Units
	2	Prof.J.A.Wakode	KOM	48	06 Units
	3	Prof.S.D.Dharmakar	MQC	48	06 Units
	4	Prof.A.S.Patil	HT	50	06 Units
	5	Prof.M.R.Kale	OE (RSM)	38	06 Units
7th Sem	1	Prof.R.T.Bharad	MTS	48	06 Units
	2	Prof.U.M.Mohod	EC-II	52	06 Units
	3	Prof.Mohd. Razik	IMC	50	06 Units
	4	Prof. A.B.Wankhade	AE	54	06 Units
	5	Prof.S.G.Bangale	PT	52	06 Units

HOD

Mechanical Engg. Dept.

Date 28/04/23

Anuradha Engineering College, Chikhli.

Department of Mechanical Engineering

Session-II (2022-23)

Syllabus Completion Report

Semester	Sr. No.	Name of Staff	Subject	No. of Lectured Conducted	Syllabus Covered
4rd Sem	1	Prof. P.S.Mansute	BEDC	52	06 Units
	2	Prof. S.S.Dharmakar	HPS	47	06 Units
	3	Prof. A.S.Patil	MS	46	06 Units
	4	Prof. A.B.Wankhade	MT	51	06 Units
	5	Prof. A.V.Deshmukh	EC-I	42	06 Units
6th Sem	1	Prof. A.M.Jumle	DOM	48	06 Units
	2	Prof.J.A.Wakode	DME	46	04 Units
	3	Prof.M.S.Sonune	CSE	46	06 Units
	4	Prof.S.S.Dharmkar	OE	40	06 Units
	5	Prof.R.T.Bharad	PE-I	40	06 Units
8th Sem	1	Prof.U.M.Mohod	RAC	52	06 Units
	2	Prof.S.S.Jadhao	ICE	51	06 Units
	3	Prof.S.G.Bangale	PPC	48	06 Units
	4	Prof.Mohd. Razik	ORT	48	06 Units

HOD

Mechanical Engg, Dept.

9. Remedial Classes Information

ANURADHA ENGINEERING COLLEGE CHIKHLI
DEPARTMENT OF MECHANICAL ENGINEERING
REMEDIAL CLASSES (2022-23)

All students are hereby informed that remedial classes are scheduled from 15 Nov 22 as per time table given below. Those students who have doubt or missed the classes could attend the remedial classes.

Time Table Incharge

H.O.D

Head of Dept.
Mechanical Engg. Dept.
Anuradha Engg. College Chikhli

ANURADHA ENGINEERING COLLEGE
DEPARTMENT OF MECHANICAL
TIME TABLE FOR REMEDIAL
Semester : FOURTH

Day /Time	10.30 - 11.30	11.30 - 12.30	01.00 - 02.00
Mon	MT AMJ	EC-I JAW	MS ASP
Tue	MS ASP	BEDC PSM	HPS SSD
Wed	MT AMJ	EC-I JAW	MS ASP
Thu	MT AMJ	BEDC PSM	HPS SSD
Fri	BEDC PSM	EC-I JAW	HPS SSD
Sat	Doubt Clearing Session		

ANURADHA ENGINEERING COLLEGE
DEPARTMENT OF MECHANICAL
TIME TABLE FOR REMEDIAL
Semester : EIGHTH

Day /Time	10.30 - 11.30	11.30 - 12.30	01.00 - 02.00
Mon	ORT MDR	ORT MDR	AE ABW
Tue	ROB DBS	AE ABW	ROB DBS
Wed	AE ABW	AE ABW	ICE UMM
Thu	ROB DBS	ROB DBS	ORT MDR
Fri	ICE UMM	ORT MDR	ICE UMM

Time-table Incharge
Dept of Mech Engg

HOD
Dept of Mech Engg

Head of Dept.
Mechanical Engg. Dept.
Anuradha Engg. College, Chikhli

ANURADHA ENGINEERING
DEPARTMENT OF MECHANICAL
TIME TABLE FOR REMEDIAL
Semester : SIXTH

Day /Time	10.30 - 11.30	11.30 - 12.30	01.00 - 02.00
Mon	CSE ASP	CSA MDR	RES ABW
Tue	FP-II SSD	CSE ASP	FP-II SSD
Wed	FP-II SSD	CSA MDR	TOM II AMJ
Thu	FP-II SSD	FP-II SSD	TOM II AMJ
Fri	CSE ASP	TOM II AMJ	RES ABW
Sat	Doubt Clearing Session		

ANURADHA ENGINEERING COLLEGE
DEPARTMENT OF MECHANICAL
TIME TABLE FOR SESSION I (2022-23)
With effect from 15 /11 / 2022

Semester : THIRD(III)

Day / Time	10.30 - 11.30	11.30 - 12.30	12.30 - 01.00	01.00 - 02.00
Mon	FM SSD	MP ABW	RECESS	M - III VRT
Tue	MOM VNJ	M - III VRT		ETD ASP
Wed	MP ABW	ETD ASP		MOM VNJ
Thu	FM SSD	MP ABW		M - III VRT
Fri	M - III VRT	ETD ASP		FM SSD
Sat	MOM VNJ	ETD ASP		MP ABW

Semester : SEVENTH (VII)

Day / Time	10.30 - 11.30	11.30 - 12.30	12.30 - 01.00	01.00 - 02.00
Mon	MTS ABW	IMC MR	RECESS	EC - II UMM
Tue	MTS ABW	IMC MR		AE ABW
Wed	PT AMJ	EC - II UMM		AE ABW
Thu	AE ABW	EC - II UMM		PT AMJ
Fri	IMC MR	PT AMJ		MTS ABW
Sat	EC - II UMM	PT AMJ		IMC MR

Time Table In Charge
(Mechanical Engg. Dept.)

HOD

Head of Dept.
Mechanical Engg. Dept.
Anuradha Engg. College, Chikhli

ANURADHA ENGINEERING COLLEGE
DEPARTMENT OF MECHANICAL
TIME TABLE FOR SESSION I (2022-23)
With effect from 15 /11 / 2022

Semester : FIFTH (V)

Day / Time	10.30 - 11.30	11.30 - 12.30	12.30 - 01.00	01.00 - 02.00
Mon	MS AMJ	HT ASP	RECESS	MQC SSD
Tue	MS AMJ	HT ASP		KOM JAW
Wed	HT ASP	MQC SSD		KOM JAW
Thu	KOM JAW	MS AMJ		HT ASP
Fri	RSM ASP	KOM JAW		HT ASP
Sat	RSM ASP	KOM JAW		MS AMJ

10.Laboratory Manual

Anuradha Engineering College, Chikhli.

Dist. - Buldana (M.S.)-443201

LAB MANUAL

Embedded System Lab

[7IT06]

Anuradha Engineering College, Chikhli

Anuradha Nagar, Sakegaon Road Chikhli

Dist. Buldana [M.S.] INDIA

Web:www.aecc.ac.in

2022-23

Paramhansa Ramkrishna Maunibaba Shikshan Sanstha's

Anuradha Engineering College, Chikhli

Anuradha Nagar, Sakegaon Road, Chikhli, Dist. Buldana

CERTIFICATE

Department of Computer Science & Engineering

This is to certify that this practical Record contains the bonafide practical work of Mr./Miss. _____
Roll No._____Class **Final Year Seventh Semester** for the subject Embedded System Lab during the academic year 2022-23

Date:____/_____/2022

Head of Department **Practical I/C**

In the absence of the above Certificate, the marks of record shall not be awarded to that examinee.

LIST OF EXPERIMENTS

2022-23

SUBJECT: Embedded System Lab **SEM: VII**

SUBJECT CODE: 7KS07 **YEAR: FINAL**

Sr. No.	Name of the Experiment	Date	Remark
1	To write a C program to demonstrate LED using 8051 Microcontroller development kit.		
2	To write a C program to demonstrate Seven Segment using 8051Microcontroller development kit		
3	To write a C program to demonstrate Traffic Light Signals using 8051 Microcontroller development kit.		
4	To write a program for demonstrating Relays and Buzzers using 8051		
5	To write a program to demonstrate Stepper Motor using 8051 Microcontroller development kit.		
6	To write a program to demonstrate LCD using 8051 Microcontroller development kit.		
7	To write a program to demonstrate Keypad using 8051 Microcontroller development kit.		
8	To Write a program to demonstrate Elevator Controller using 8051 microcontroller development kit.		

OVERVIEW OF EMBEDDED SYSTEMS

AT89C51 MICROCONTROLLER

FEATURES

- 80C51 based architecture
- 4-Kbytes of on-chip Reprogrammable Flash Memory
- 128 x 8 RAM
- Two 16-bit Timer/Counters
- Full duplex serial channel
- Boolean processor
- Four 8-bit I/O ports, 32 I/O lines
- Memory addressing capability
  - 64K ROM and 64K RAM
- Power save modes:
  - Idle and power-down
- Six interrupt sources
- Most instructions execute in 0.3 us
- CMOS and TTL compatible
- Maximum speed: 40 MHz @ Vcc = 5V
- Industrial temperature available
- Packages available:

– 40-pin DIP

– 44-pin PLCC

– 44-pin PQFP

GENERAL DESCRIPTION:

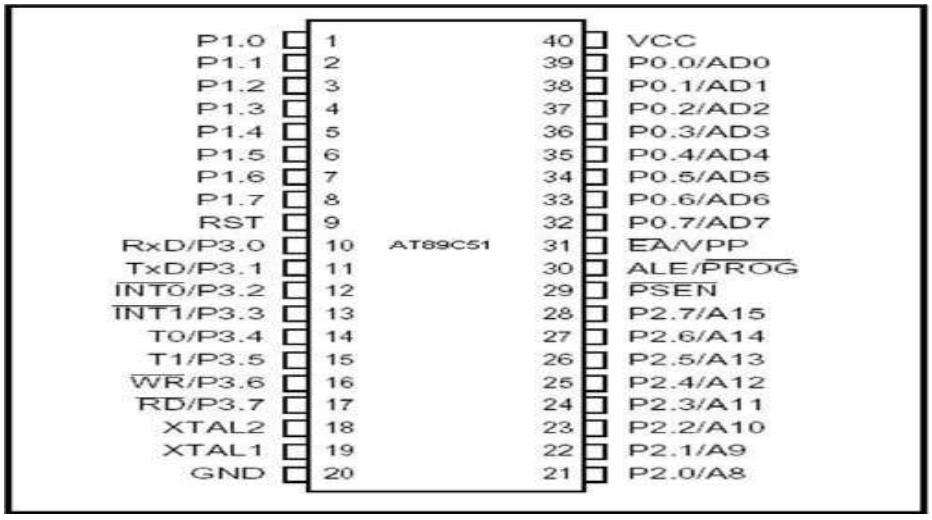
THE MICROCONTROLLER:

A microcontroller is a general purpose device, but that is meant to read data, perform limited calculations on that data and control its environment based on those calculations. The prime use of a microcontroller is to control the operation of a machine using a fixed program that is stored in ROM and that does not change over the lifetime of the system.

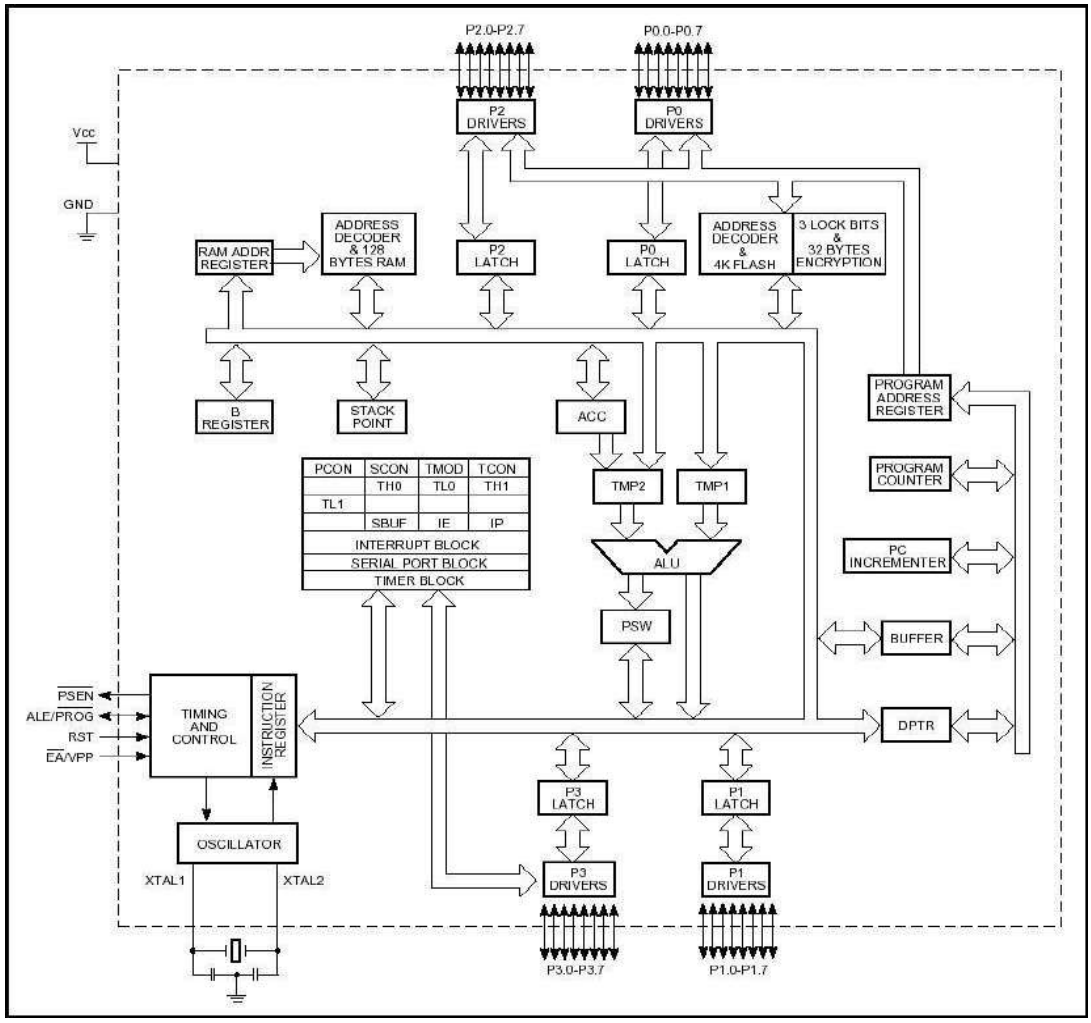
The microcontroller design uses a much more limited set of single and double byte instructions that are used to move data and code from internal memory to the ALU. The microcontroller is concerned with getting data from and to its own pins; the architecture and instruction set are optimized to handle data in bit and byte size.

The AT89C51 is a low-power, high-performance CMOS 8-bit microcontroller with 4k bytes of Flash Programmable and erasable read only memory (EROM). The device is manufactured using Atmel‟s high-density nonvolatile memory technology and is functionally compatible with the industry-standard 80C51 microcontroller instruction set and pin out. By combining versatile 8-bit CPU with Flash on a monolithic chip, the Atmel‟s AT89c51 is a powerful microcomputer, which provides a high flexible and cost- effective solution to many embedded control applications.

Pin configuration of AT89c51 Microcontroller



AT89C51 Block Diagram



PIN DESCRIPTION:

VCC-Supply voltage

GND-Ground

Port 0

Port 0 is an 8-bit open drain bi-directional I/O port. As an output port, each pin can sink eight TTL inputs. When 1s are written to port 0 pins, the pins can be used as high impedance inputs.

Port 0 can also be configured to be the multiplexed low order address/data bus during access to external program and data memory. In this mode, P 0 has internal pull-ups. Port 0 also receives the code bytes during Flash programming and outputs the code bytes during program verification. External pull-ups are required during program verification.

Port 1

Port 1 is an 8-bit bi-directional I/O port with internal pull-ups. The port 1output buffers can sink/source four TTL inputs. When 1s are written to port 1 pins, they are pulled high by the internal pull-ups can be used as inputs. As inputs, Port 1 pins that are externally being pulled low will source current (1) because of the internal pull-ups.

Port 2

Port 2 is an 8-bit bi-directional I/O port with internal pull-ups. The port 2 output buffers can sink/source four TTL inputs. When 1s are written to port 2 pins, they are pulled high by the internal pull-ups can be used as inputs. As inputs, Port 2 pins that are externally being pulled low will source current because of the internal pull-ups.

Port 2 emits the high-order address byte during fetches from external program memory and during access to DPTR. In this application Port 2 uses strong internal pull-ups when emitting 1s. During accesses to external data memory that use 8-bit data address (MOVX@R1), Port 2 emits the contents of the P2 Special Function Register. Port 2 also receives the high-order address bits and some control signals during Flash programming and verification.

Port 3

Port 3 is an 8-bit bi-directional I/O port with internal pull-ups. The port 3 output buffers can sink/source four TTL inputs. When 1s are written to port 3 pins, they are pulled high by the internal pull-ups can be used as inputs. As inputs, Port 3 pins that are externally being pulled low will source current because of the internal pull-ups.

Port 3 also receives some control signals for Flash Programming and verification.

Port pin	Alternate Functions
P3.0	RXD(serial input port)
P3.1	TXD(serial input port)
P3.2	INT0(external interrupt 0)
P3.3	INT1(external interrupt 1)
P3.4	T0(timer 0 external input)
P3.5	T1(timer 1 external input)
P3.6	WR(external data memory write strobe)
P3.7	RD(external data memory read strobe)

RST

Rest input A on this pin for two machine cycles while the oscillator is running resets the device.

ALE/PROG:

Address Latch Enable is an output pulse for latching the low byte of the address during access to external memory. This pin is also the program pulse input (PROG) during Flash programming.

In normal operation ALE is emitted at a constant rate of 1/16 the oscillator frequency and may be used for external timing or clocking purpose. Note, however, that one ALE pulse is skipped during each access to external Data memory.

PSEN

Program Store Enable is the read strobe to external program memory when the AT89c51 is executing code from external program memory PSEN is activated twice each machine cycle, except that two PSEN activations are skipped during each access to external data memory.

EA /VPP

External Access Enable (EA) must be strapped to GND in order to enable the device to fetch code from external program memory locations starting at 0000h up to FFFFH. Note, however, that if lock bit 1 is programmed EA will be internally latched on reset. EA should be strapped to Vcc for internal program executions. This pin also receives the 12-volt programming enable voltage (Vpp) during Flash programming when 12-volt programming is selected.

XTAL1

Input to the inverting oscillator amplifier and input to the internal clock operating circuit.

XTAL 2

Output from the inverting oscillator amplifier.

OPERATING DESCRIPTION

The detail description of the AT89C51 included in this description is:

• Memory Map and Registers

• Timer/Counters

• Interrupt System

MEMORY MAP AND REGISTERS:

Memory

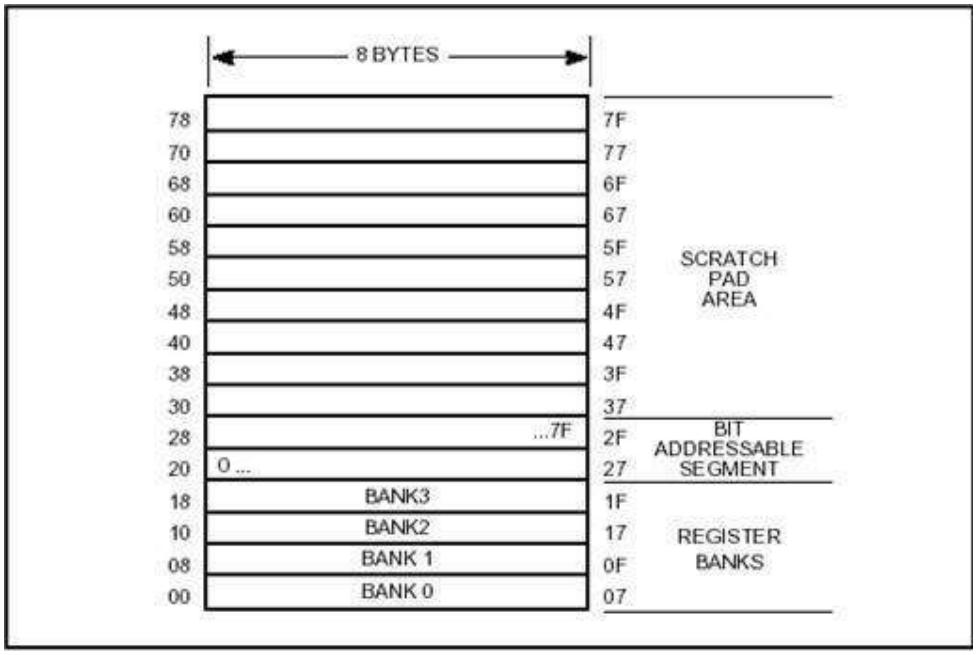
The AT89C51 has separate address spaces for program and data memory. The program and data memory can be up to 64K bytes long. The lower 4K program memory can reside on-chip. The AT89C51 has 128 bytes of on-chip RAM.

The lower 128 bytes can be accessed either by direct addressing or by indirect addressing. The lower 128 bytes of RAM can be divided into 3 segments as listed below

1. **Register Banks 0-3:** locations 00H through 1FH (32 bytes). The device after reset defaults to register bank 0. To use the other register banks, the user must select them in software. Each register bank contains eight 1-byte registers R0-R7. Reset initializes the stack point to location 07H, and is incremented once to start from 08H, which is the first register of the second register bank.

2. **Bit Addressable Area:** 16 bytes have been assigned for this segment 20H-2FH. Each one of the 128 bits of this segment can be directly addressed (0-7FH). Each of the 16 bytes in this segment can also be addressed as a byte.

3. **Scratch Pad Area:** 30H-7FH are available to the user as data RAM. However, if the data pointer has been initialized to this area, enough bytes should be left aside to prevent SP data destruction.



SPECIAL FUNCTION REGISTERS:

The Special Function Registers (SFR's) are located in upper 128 Bytes direct addressing area. The SFR Memory Map in shows that.

Not all of the addresses are occupied. Unoccupied addresses are not implemented on the chip. Read accesses to these addresses in general return random data, and write accesses have no effect. User software should not write 1s to these unimplemented locations, since they may be used in future microcontrollers to invoke new features. In that case, the reset or inactive values of the new bits will always be 0, and their active values will be 1.

The functions of the SFR"s are outlined in the following sections.

Accumulator (ACC)

ACC is the Accumulator register. The mnemonics for Accumulator-specific instructions, however, refer to the Accumulator simply as A.

B Register (B)

The B register is used during multiply and divide operations. For other instructions it can be treated as another scratch pad register.

Program Status Word (PSW)

The PSW register contains program status information.

Stack Pointer (SP)

The Stack Pointer Register is eight bits wide. It is incremented before data is stored during PUSH and CALL executions. While the stack may reside anywhere in on chip RAM, the Stack Pointer is initialized to 07H after a reset. This causes the stack to begin at location 08H.

Data Pointer (DPTR)

The Data Pointer consists of a high byte (DPH) and a low byte (DPL). Its function is to hold a 16-bit address. It may be manipulated as a 16-bit register or as two independent 8-bit registers.

Serial Data Buffer (SBUF)

The Serial Data Buffer is actually two separate registers, a transmit buffer and a receive buffer register. When data is moved to SBUF, it goes to the transmit buffer, where it is held for serial transmission. (Moving a byte to SBUF initiates the transmission.) When data is moved from SBUF, it comes from the receive buffer.

Timer Registers

Register pairs (TH0, TL0) and (TH1, TL1) are the 16-bit Counter registers for Timer/Counters 0 and 1, respectively.

Control Registers

Special Function Registers IP, IE, TMOD, TCON, SCON, and PCON contain control and status bits for the interrupt system, the Timer/Counters, and the serial port.

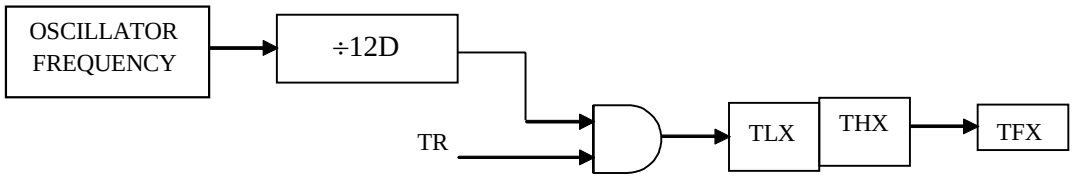
TIMER / COUNTERS:

The IS89C51 has two 16-bit Timer/Counter registers: Timer 0 and Timer 1. All two can be configured to operate either as Timers or event counters. As a Timer, the register is incremented every machine cycle. Thus, the register counts machine cycles. Since a machine cycle consists of 12 oscillator periods, the count rate is 1/12 of the oscillator frequency.

As a Counter, the register is incremented in response to a 1-to-0 transition at its corresponding external input pin, T0 and T1. The external input is sampled during S5P2 of every machine cycle. When the samples show a high in one cycle and a low in the next cycle, the count is incremented. The new count value appears in the register during S3P1 of the cycle following the one in which the transition was detected. Since two machine cycles (24 oscillator periods) are required to recognize a 1-to-0 transition, the maximum count rate is 1/24 of the oscillator frequency. There are no restrictions on the duty cycle of the external input signal, but it should be held for at least one full machine cycle to ensure that a given level is sampled at least once before it changes.

In addition to the Timer or Counter functions, Timer 0 and Timer 1 have four operating modes: 13-bit timer, 16-bit timer, 8-bit auto-reload, split timer.

TIMERS:



SFR'S USED IN TIMERS

The special function registers used in timers are,

- TMOD Register
- TCON Register
- Timer(T0) & timer(T1) Registers

(i) TMOD Register:

TMOD is dedicated solely to the two timers (T0 & T1).

- The timer mode SFR is used to configure the mode of operation of each of the two timers. Using this SFR your program may configure each timer to be a 16-bit timer, or 13 bit timer, 8-bit auto reload timer, or two separate timers. Additionally you may configure the timers to only count when an external pin is activated or to count "events" that are indicated on an external pin.
- It can consider as two duplicate 4-bit registers, each of which controls the action of one of the timers.

(ii) TCON Register:

- The timer control SFR is used to configure and modify the way in which the 8051"s two timers operate. This SFR controls whether each of the two timers is running or stopped and contains a flag to indicate that each timer has overflowed. Additionally, some non-timer related bits are located in TCON SFR.
- These bits are used to configure the way in which the external interrupt flags are activated, which are set when an external interrupt occurs.

TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0

(iii) TIMER 0 (T0):

- TO (Timer 0 low/high, address 8A/8C h)

  These two SFR"s taken together represent timer 0. Their exact behavior depends on how the timer is configured in the TMOD SFR; however, these timers always count up. What is configurable is how and when they increment in value.

TH0	TL0

(iv) TIMER 1 (T1):

- T1 (Timer 1 Low/High, address 8B/ 8D h)

These two SFR"s, taken together, represent timer 1. Their exact behavior depends on how the timer is configured in the TMOD SFR; however, these timers always count up. What is Configurable is how and when they increment in value.

TH1	TL1

The Timer or Counter function is selected by control bits C/T in the Special Function Register TMOD. These two Timer/Counters have four operating modes, which are selected by bit pairs (M1, M0) in TMOD. Modes 0, 1, and 2 are the same for both Timer/Counters, but Mode 3 is different.

The **FOUR** modes are described in the following sections:

Mode 0:

Both Timers in Mode 0 are 8-bit Counters with a divide-by-32 pre scalar. Figure 8 shows the Mode 0 operation as it applies to Timer 1. In this mode, the Timer register is configured as a 13-bit register. As the count rolls over from all 1s to all 0s, it sets the Timer interrupt flag TF1. The counted input is enabled to the Timer when TR1 = 1 and either GATE = 0 or INT1 = 1. Setting GATE = 1 allows the Timer to be controlled by external input INT1, to facilitate pulse width measurements. TR1 is a control bit in the Special Function Register TCON. Gate is in TMOD.

The 13-bit register consists of all eight bits of TH1 and the lower five bits of TL1. The upper three bits of TL1 are indeterminate and should be ignored. Setting the run flag (TR1) does not clear the registers.

Mode 0 operation is the same for Timer 0 as for Timer 1, except that TR0, TF0 and INT0 replace the corresponding Timer 1 signals. There are two different GATE bits, one for Timer 1 (TMOD.7) and one for Timer 0 (TMOD.3).

Mode 1

Mode 1 is the same as Mode 0, except that the Timer register is run with all 16 bits. The clock is applied to the combined high and low timer registers (TL1/TH1). As clock pulses are received, the timer counts up: 0000H, 0001H, 0002H, etc. An overflow occurs on the FFFFH-to-0000H overflow flag. The timer continues to count. The overflow flag is the TF1 bit in TCON that is read or written by software

Mode 2

Mode 2 configures the Timer register as an 8-bit Counter (TL1) with automatic reload, as shown in Figure 10. Overflow from TL1 not only sets TF1, but also reloads TL1 with the contents of TH1, which is preset by software. The reload leaves the TH1 unchanged. Mode 2 operation is the same for Timer/Counter 0.

Mode 3

Timer 1 in Mode 3 simply holds its count. The effect is the same as setting TR1 = 0. Timer 0 in Mode 3 establishes TL0and TH0 as two separate counters. The logic for Mode 3 on Timer 0 is shown in Figure 11. TL0 uses the Timer 0 control bits: C/T, GATE, TR0, INT0, and TF0. TH0 is locked into a timer function (counting machine cycles) and over the use of TR1 and TF1 from Timer 1. Thus, TH0 now controls the Timer 1 interrupt.

Mode 3 is for applications requiring an extra 8-bit timer or counter. With Timer 0 in Mode 3, the AT89C51 can appear to have three Timer/Counters. When Timer 0 is in Mode 3, Timer 1 can be turned on and off by switching it out of and into its own Mode 3. In this case, Timer 1 can still be used by the serial port as a baud rate generator or in any application not requiring an interrupt.

INTERRUPT SYSTEM

An interrupt is an external or internal event that suspends the operation of micro controller to inform it that a device needs its service. In interrupt method, whenever any device needs its service, the device notifies the micro controller by sending it an interrupt signal. Upon receiving an interrupt signal, the micro controller interrupts whatever it is doing and serves the device. The program associated with interrupt is called as **interrupt service subroutine (ISR**).Main advantage with interrupts is that the micro controller can serve many devices.

Baud Rate

The baud rate in Mode 0 is fixed as shown in the following equation. Mode 0 Baud Rate = Oscillator Frequency /12 the baud rate in Mode 2 depends on the value of the SMOD bit in Special Function Register PCON. If SMOD = 0 the baud rate is 1/64 of the oscillator frequency.

If SMOD = 1, the baud rate is 1/32 of the oscillator frequency.

Mode 2 Baud Rate = 2SMODx (Oscillator Frequency)/64.

In the IS89C51, the Timer 1 overflow rate determines the baud rates in Modes 1 and 3.

NUMBER OF INTERRUPTS IN 89C51:

There are basically five interrupts available to the user. Reset is also considered as an interrupt. There are two interrupts for timer, two interrupts for external hardware interrupt and one interrupt for serial communication.

Memory location	Interrupt name
0000H	Reset
0003H	External interrupt 0
000BH	Timer interrupt 0
0013H	External interrupt 1
001BH	Timer interrupt 1
0023H	Serial COM interrupt

Lower the vector, higher the priority. The External Interrupts INT0 and INT1 can each be either level-activated or transition-activated, depending on bits IT0 and IT1 in Register TCON. The flags that actually generate these interrupts are the IE0 and IE1 bits in TCON. When the service routine is vectored, hardware clears the flag that generated an external interrupt only if the interrupt was transition-activated. If the interrupt was level-activated, then the external requesting source (rather than the on-chip hardware) controls the request flag.

The Timer 0 and Timer 1 Interrupts are generated by TF0and TF1, which are set by a rollover in their respective Timer/Counter registers (except for Timer 0 in Mode 3).When a timer interrupt is generated, the on-chip hardware clears the flag that is generated.

The Serial Port Interrupt is generated by the logical OR of RI and TI. The service routine normally must determine whether RI or TI generated the interrupt, and the bit must be cleared in software.

All of the bits that generate interrupts can be set or cleared by software, with the same result as though they had been set or cleared by hardware. That is, interrupts can be generated and pending interrupts can be canceled in software.

Each of these interrupt sources can be individually enabled or disabled by setting or clearing a bit in Special Function Register IE (interrupt enable) at address 0A8H. There is a global enable/disable bit that is cleared to disable all interrupts or to set the interrupts.

IE (Interrupt enable register):

Steps in enabling an interrupt:

Bit D7 of the IE register must be set to high to allow the rest of register to take effect. If EA=1, interrupts are enabled and will be responded to if their corresponding bits in IE are high. If EA=0, no interrupt will be responded to even if the associated bit in the IE register is high.

Description of each bit in IE register:

D7 bit: Disables all interrupts. If EA =0, no interrupt is acknowledged, if EA=1 each interrupt source is individually enabled or disabled by setting or clearing its enable bit.

- D6 bit: Reserved.
- D5 bit: Enables or disables timer 2 over flow interrupt (in 8052).
- D4 bit: Enables or disables serial port interrupt.
- D3 bit: Enables or disables timer 1 over flow interrupt.
- D2 bit: Enables or disables external interrupt 1.
- D1 bit: Enables or disables timer 0 over flow interrupt.
- D0 bit: Enables or disables external interrupt 0.

Interrupt priority in 89C51:

There is one more SRF to assign priority to the interrupts which is named as interrupt priority (IP). User has given the provision to assign priority to one interrupt. Writing one to that particular bit in the IP register fulfils the task of assigning the priority.

Description of each bit in IP register:

D7 bit: Reserved.

D6 bit: Reserved.

D5 bit: Timer 2 interrupt priority bit (in 8052).

D4 bit: Serial port interrupt priority bit.

D3 bit: Timer 1 interrupt priority bit.

D2 bit: External interrupt 1 priority bit.

D1 bit: Timer 0 interrupt priority bit.

D0 bit: External interrupt 0 priority bit

8051 CORE MICRO CONTROLER:

General Description

8051 is a high performance microcontroller fabricated using CMOS technology. 8051 is an 8-Bit Micro Controller with 4-Kbytes of Flash memory, 128 Bytes On-chip RAM, 32 programmable I/O Lines, two 16-bit Timers/Counters, 6 Interrupts/2 Priority Levels, UART and an on-chip oscillator and clock circuit. The AT89S52 can be expanded using standard TTL compatible memory.

FEATURES OF KIT

- 8051 based architecture
- 4-Kbytes of on-chip Reprogrammable Flash Memory
- 256 x 8 RAM
- Two 16-bit Timer/Counters
- Full duplex serial channel
- Boolean processor
- Four 8-bit I/O ports, 32 I/O lines
- Memory addressing capability 64K ROM and 64K RAM
- Program memory lock: Lock bits (3)
- Power save modes: Idle and power-down
- Six interrupt sources
- CMOS and TTL compatible
- Maximum speed: 40 MHz @ Vcc = 5V
- Packages available: 40-pin DIP, 44-pin PLCC, 44-pin PQFP

FEATURES OF DEVELOPMENT BOARD

- In-System programming (ISP) facility for supported microcontrollers
- 16 x 2 Character LCD Display
- On board RS-232 compatible serial interface terminated in a 9 pin „D" female
- Connector.
- One Temperature sensor (LM35).
- I2C EEPROM (AT 24C16) for storing non-volatile parameters
- I2C Real Time Clock (DS1307) with Lithium battery and SRAM
- I2C 4-Channel (8–Bit) A/D converter
- I2C 1-Channel (8-Bit) D/A Converter
- 4 x 4 Matrix Keypad (optional)

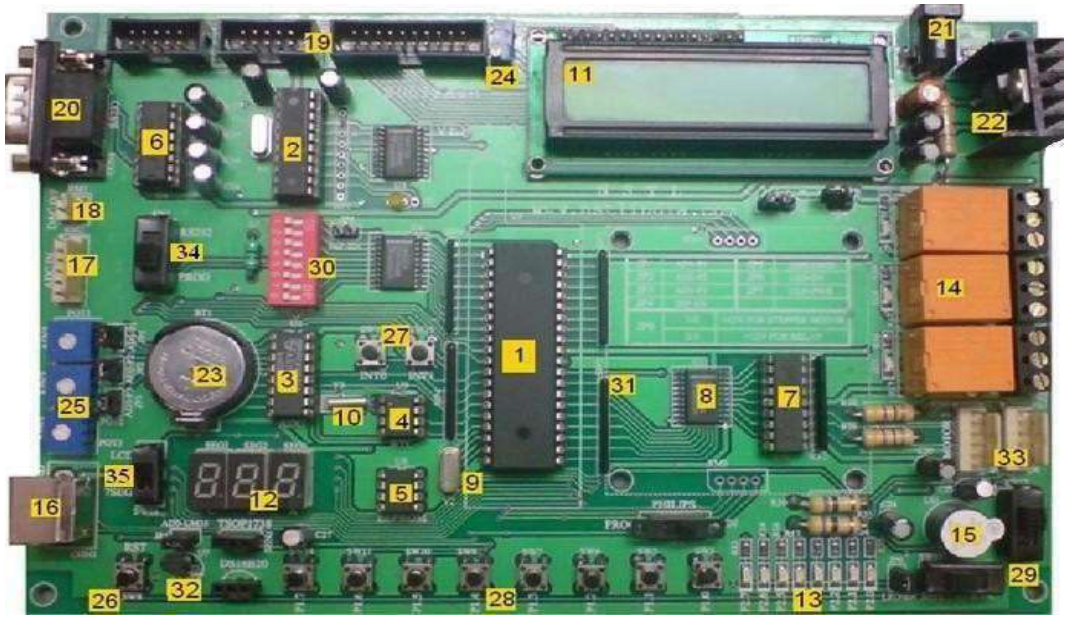
- 8 Push - to - on switches
- Standard AT keyboard Interface
- Two External Interrupts
- Three 7-Segment LED Displays
- 8-high current output pins (500mA) for driving external loads
- Stepper Motor Interfacing
- Supports up to 16 different Micro Controllers of 8051 and AVR Family

ADD ON MODULES

- 4 x 4 KEYPAD
- STEPPERMOTOR
- DS1820 (temperature sensor)
- TSOP1738 (38KHz IR-Receiver)

COMPONENTS

1. AT89S52 (40 PIN DIP)
2. AT89C2051 (ISP)
3. PCF8591 (ADC/DAC)
4. RTC
5. EEPROM
6. MAX 232
7. ULN 2803
8. 74HC573 LATCH (3- ICS)
9. CRYSTAL (11.0592MHZ)
10. CRYSTAL (32.768KHZ)
11. LCD (16X2 PIN CONNECTOR)
12. 7-Segment Display
13. SMD LEDS (8)
14. RELAYS (3)
15. Buzzer
16. PS2 CONNECTOR
17. 6 PIN RELEVENT CONNECTORS
18. 2-PIN RELEVENT CONNECTORS
19. 20 PIN, 10 PIN (2) CONNECTORS
20. DB9 CONNECTOR
21. DC SOCKET
22. 7805 REGULATOR
23. Battery
24. 10K POT (1 for LCD)
25. 10K POTS (3 for ADC)
26. RESET SWITCH (1)
27. INTERRUPT SWITCHES (2)
28. KEYPAD SWITCHES (8)
29. Switches (3)
30. DIP Switches
31. 4.7K RESISTORS (PULL UP RESISTORS)
32. LM-35 (Temperature sensor)
33. STEPPER MOTOR CONNECTORS (2)
34. RS232 or PROG mode switch
35. LCD or 7SEGMENT mode switch



Power supply

A 12V/1A DC power adapter is required to power the 8051 Starter kit. The power output from this adapter is supplied to LM7805 voltage regulator, which gives the constant 5V DC to the starter kit. Capacitors at the output take care of surge current. A few decoupling ceramic capacitors have also been placed around the board.

Address Table:

Device	Address (16-bit)
LCD_EN	0x8000
ADC	0x8400
Key Pad	0x8200
LED‟s	0x8600
4 x 4 Key Pad	0x8100
Stepper Motor	0x8500
7-Segment Display	0x8C00
DAC	0x8800
LCD Command Write	0x8000
LCD Check	0x8002
LCD Data Write	0x8001

7-Segment LED's Selection:

Device	Address (16-Bit)
7-Segment LED1	0x8C03
7-Segment LED2	0x8C05
7-Segment LED3	0x8C06

ADC PINS

PINS	**Address(16-bit)**
ADC_START	0x8B00
ADC_ALE	0x8F00

PROGRAM 1
LED

Program Description

In this program we try to glow all seven LED"s in different formats (from L → R , R → L , even , odd). Initialize with LED address.For LED"s to glow from Right to Left (R → L) one after the the other set the counter c=0 and increment the counter by one till the value reaches c=7and in between call set and clear LED function. LED"s glow from Left to Right (L → R) one after the the other). Initialize with LED address. For LED"s to glow from Right to Left (R → L) one after the the other set the counter c=7 and decrement the counter by one till the value reaches c=0and in between call set and clear LED function.

PROGRAM FOR EXAMPLE OF LED:

```
#include<REGX51.H>
#define LED P2
void delay(unsigned int d);
int main(void)
{
        while(1)
        {
                LED=0x55;
                delay(1000);
                LED=0xAA;
                delay(1000);
        }
}
void delay(unsigned int d)
{
        unsigned int i,j;
        for(i=0; i<d; i++)
        for(j=0; j>101 ;j++);
}
```

PROGRAM TO SHOW L-R & R-L SHIFTING:

```
#include<REGX51.H>
#define LED P2
void delay(unsigned   int d);
int main(void)
{
unsigned int i;
```

```
while(1)
{
        LED=0X01;
        for(i=0;i<7;i++)
        {
                delay(1000);
                LED=LED<<=0X01;
        }
        LED=0X80;
        for(i=0;i<=7;i++)
        {
                delay(1000);
                LED=LED>>=0X01;
        }}}
void delay(unsigned int d)
{
        unsigned i,j;
        for(i=0;i<d;i++)
        for(j=0;j<101;j++);
}
```

Program Validation

Input:
Initialize with LED address.For LED‟s to glow from Right to Left (R → L) one after the the other set the counter c=0 and increment the counter by one till the value reaches c=7.

Output:
LED‟s to glow from Right to Left (R → L) one after other.

LED EXAMPLE:

L-R7R-L SHIFT:

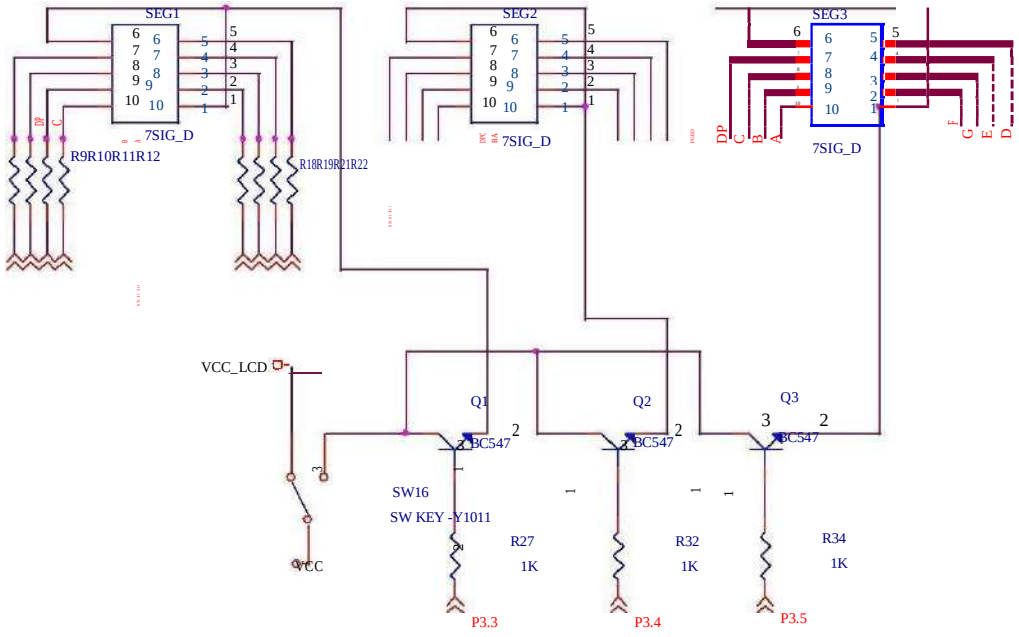
Conclusion:

The C program to demonstrate LED was executed successfully using 8051 Microcontroller development kit.

PROGRAM 2
SEVEN SEGMENT DISPLAY

Three Seven segment display are connected to port0 and the common anode pins of each seven segment are connected to port 3.3, 3.4 and 3.5 respectively. And the same port0 is connected to LCD as well, so to avoid the conflict we have provided the slide switch to select the appropriate display.

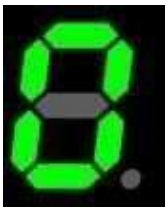
Schematic of Seven Segment Display:



General Description:

A seven segment display, as its name indicates, is composed of seven elements. Individually on or off, they can be combined to produce simplified representations of the Hindu _Arabic numerals. Often the seven segments are arranged in an *oblique*, or italic, arrangement, which aids readability. Each of the numbers 0, 1, 2 and 9 may be represented by two or more different glyphs on seven-segment displays. LED-based 7-segment display showing the 16 hex digits

The seven segments are arranged as a rectangle of two vertical segments on each side with one horizontal segment on the top and bottom. Additionally, the seventh segment bisects the rectangle horizontally. There are also fourteen –segment displays and sixteen segment displays (for full alphanumeric); however, these have mostly been replaced by dot-matrix displays. The segments of a 7-segment display are referred to by the letters A to G, as shown to the right, where the optional DP (decimal point an "eighth segment") is used for the display of non-integer numbers.



It is an image sequence of a "LED" display, which is described technology-wise in the following section. Notice the variation between uppercase and lowercase letters for A–F; this is done to obtain a unique, unambiguous shape for each letter.

ALGORITHM:

STEP1: Configure the Hardware connections of 7-SEGMENT devices

STEP2: Load the data on the port0 and enable 7-Seg1.

STEP3: Load the data on the port0 and enable 7-Seg2.

STEP4**:** Load the data on the port0 and enable 7-Seg3.

STEP5: End

PROGRAM TO INTERFACE 7 SEGMENT DISPLAY:

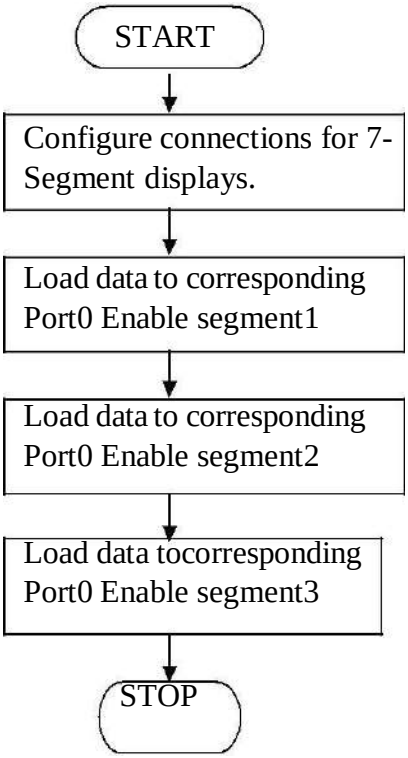
```
#include<REGX51.H>
#define SEG1 {P3_3=0;P3_4=0;P3_5=1;}
#define SEG2 {P3_3=0;P3_4=1;P3_5=0;}
#define SEG3 {P3_3=1;P3_4=0;P3_5=0;}
#define NULL {P3_3=0;P3_4=0;P3_5=0;}

code unsigned char seg[10]={0xc0,0xf9,0xa4,0xb0,0x99,0x92,0x82,0xf8,0x80,0x90};
int main(void)
{
        unsigned char i,j,k,m;
        unsigned int l;
        for(i=0;i<10;i++)
        {
                for(j=0;j<10;j++)
                {
                for(k=0;k<10;k++)
                {
                for(l=0;l<1000;l++)
                {
                        NULL
                        P0=seg[i];
                         SEG1
                         for(m=0;m<50;m++);

                        NULL
                         P0=seg[j];
                         SEG2
                        for(m=0;m<50;m++);

                        NULL
                        P0=seg[k];
                        SEG3
                        for(m=0;m<50;m++);
                }
         }}}
         }
```

FLOW CHART:



Conclusion:

The C program to demonstrate LED SEVEN SEGMENT DISPLAY was executed successfully using 8051 Microcontroller development kit.

PROGRAM 3
TRAFFIC LIGHT SIGNALS

Program Definition

To write a C program to demonstrate Traffic Light signals using 8051 Microcontroller development kit.

Program Description

We demonstrate traffic signals i.e, all the possible ways where in flow of opposite directions is allowed and also free lefts. Writing hex code for traffic control combinations, we send data as (traffic light hex code) to LED address example led(0x**99**) then delay for some time , Again send other combination as data to LED

Algorithm:

1. Assign LED address for Microcontroller kit.
2. While true.
3. Write data (traffic light hex code) to LED address.
4. Delay for certain time.
5. Provide other possible ways to LED address.
6. Delay for certain time.
7. Repeat step 5 with different combination.

PROGRAM FOR TRAFFIC CONTROLLER:

```
#include<REGX51.H>
void delay (unsigned int d);
int main(void)
        {
        while(1)
                {
                P2=0x54;
                delay(500);
                P2=0x56;
                delay(500);
                P2=0x51;
                delay(500);
                P2=0x59;
```

```
                delay(500);
                P2=0x45;
                delay(500);
                P2=0x65;
                delay(500);
                P2=0x15;
                delay(500);
                P2=0x95;
                delay(500);
                }
        }
void delay (unsigned int d)
{
        unsigned int i,j;
        for(i=0;i<d;i++)
        for(j<0;j<101;j++);
}
```

Program Validation

Input

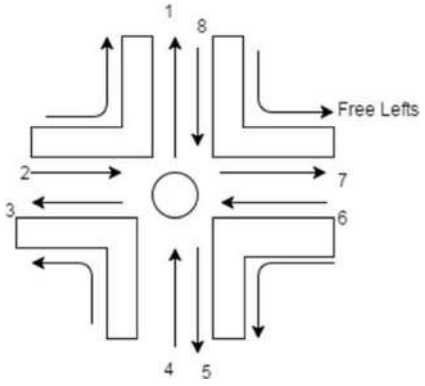
First making the LED"s 1,4,5,8 as „1" & others as „0" then converting into decimal

eg: 1 4 5 8

```
8 7 6 5  4 3 2 1
1 0 0 1 1 0 0 1
  ↓       ↓
  9       9
```

Now, we send data as led(0x**99)**

Output



Conclusion:

The C program to demonstrate Traffic controller was executed successfully using 8051 Microcontroller development kit.

PROGRAM 4
RELAY AND BUZZER

Program Definition

To write a program for demonstrating Relays Buzzer using 8051 development kit.

Program Description

RELAY

We demonstrate glowing of 2 relays one after the other . A relay is a device that responds to a small current or voltage change by activating switches or other devices in an electric circuit. Used for alarming systems.

Ports on MP:

7 6 5 4	3 2	1 0
↓	↓	↓
Stepper-Motor	Buzzer	Relay

Relay 1:

Prev=Prev | (1<< **0**) (*for glowing)* , Prev=Prev & ~(1<< **0**) *(for clearing)*

Relay2 :

Prev=Prev | (1<< **1**) (*for glowing)* , Prev=Prev & ~(1<< **1**) *(for clearing)*

Algorithm

1. Assign LED address for Microcontroller kit
2. While true
3. Set the first relay to 1 which indicates that it is “ON”
4. Delay for certain time.
5. Set the relay to 0 which is “OFF”
6. Delay for certain time.
7. Set the realy2 to „1“
8. Delay for certain time.
9. Set the relay2 to „0“
10. Delay for certain time.

Program Description Buzzer

We demonstrate buzzing of two Buzzers. A **Buzzer** an electrical device that makes a buzzing noise and is used for signaling.

Ports on MP:

7 6 5 4	3 2	1 0
↓	↓	↓

Stepper-Motor Buzzer Relay

For 1st Buzzer:

Set Buzzer: Prev=Prev | (1<< 2) Reset Buzzer: Prev=Prev & ~(1<< 2)

For 2nd Buzzer:

Set Buzzer: Prev=Prev | (1<< 3) Reset Buzzer: Prev=Prev & ~(1<< 3)

Algorithm

1. Assign LED address for Microcontroller kit.
2. While true.
3. Set the first buzzer to 1 which indicates that it is “ON”.
4. Delay for certain time.
5. Set the buzzer to 0 which is “OFF”
6. Delay for certain time.
7. Set the buzzer2 to „1“
8. Delay for certain time.
9. Set the buzzer2 to „0“
10. Delay for certain time.

PROGRAM TO INTERFACE RELAY AND BUZZER:

```
#include<REGX51.H>
#define RELAY1 P2_4
#define RELAY2 P2_5
#define RELAY3 P2_6
#define BUZZER P2_7
void delay(unsigned int d);
int main(void)
{
        P2=0x00;
        while(1)
        {
                RELAY1=1;
                delay(1000);
                RELAY1=0;
                delay(1000);
                RELAY2=1;
                delay(1000);
                RELAY2=0;
```

```
                delay(1000);

                RELAY3=1;
                delay(1000);
                RELAY3=0;
                delay(1000);
                BUZZER=1;
                delay(1000);
                BUZZER=0;
                delay(1000);
        }
}

void delay(unsigned int d)
{
        unsigned int i,j;
        for(i=0;i<d;i++)
        for(j=0;j<101;j++);
}
```

Program Validation

Input for Relay:

Set the first relay to 1 which indicates that it is “ON”
Set the relay to 0 which is “OFF”
Set the realy2 to „1“ which indicates that it is “ON”
Set the relay2 to „0“ which is “OFF”

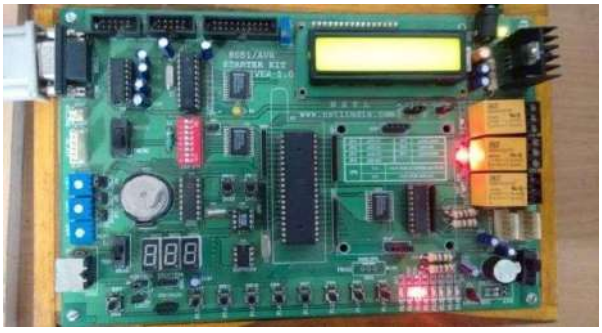
Input for Buzzer:

Set the first Buzzer1 to 1 which indicates that it is “ON”
Set the Buzzer1 to 0 which is “OFF”
Set the Buzzer2 to „1“ which indicates that it is “ON”
Set the Buzzer2 to „0“ which is “OFF”

Output :

Here two Relays glow one after the other.

RELAYS AND BUZZER:



Conclusion:

The C program to demonstrate Relays & Buzzer was executed successfully using 8051 Microcontroller development kit.

Program 5
STEPPER MOTOR

Program Definition

To write a program to demonstrate Stepper Motor using 8051 development kit.

Basics of Stepper Motor

Of all motors, step motor is the easiest to control. Direction information is very simple and comes down to "left" for logical one on that pin and "right" for logical zero. Motor control is also very simple - every impulse makes the motor operating for one step and if there is no impulse the motor won't start. Pause between impulses can be shorter or longer and it defines revolution rate. This rate cannot be infinite because the motor won't be able to "catch up" with all the impulses.

The key to driving a stepper is realizing how the motor is constructed. A diagram shows the representation of a 4 coil motor, so named because 4 coils are used to cause the revolution of the drive shaft. Each coil must be energized in the correct order for the motor to spin.

The control signals to open and close the switches at the appropriate times in order to spin the motors. The control unit is commonly a computer or programmable interface controller, with software directly generating the outputs needed to control the switches.

Step angle: It is angle through which motor shaft rotates in one step. step angle is different for different motor . Selection of motor according to step angle depends on the application, simply if you require small increments in rotation choose motor having smaller step angle.

No of steps require to rotate one complete rotation = 360 deg. / step angle in deg.

Steps/second
The relation between RPM and steps per sec. is given by, steps or impulses /sec. = (RPM X Steps /revolution) /60

Interfacing To 8051

Coil A	Coil B	Coil C	Coil D	Step
0	1	1	0	1
0	0	1	1	2
1	0	0	1	3
1	1	0	0	4

To cause the stepper to rotate, we have to send a pulse to each coil in turn. The 8051 does not have sufficient drive capability on its output to drive each coil, so there are a number of ways to drive a stepper, Stepper motors are usually controlled by transistor or driver IC like ULN2003.

Driving current for each coil is then needed about 60mA at +5V supply. A Darlington transistor array, ULN2003 is used to increase driving capacity of the 8051 chip. Four 4.7k resistors help the 8051 to provide more sourcing current from the +5V supply.

Controlling Stepper Motor With Two Port Pins Only

D0	D0	Coil energized
0	0	AB
0	1	BC
1	0	CD
1	1	DA

Program Description

Demonstrate "Stepper Motor " rotating in clockwise and anticlockwise direction. A stepper motor or step motor or stepping motor is a brushless DC electric motor that divides a full rotation into a number of equal steps.

We consider 10H-16
20H-32
40H-64
80H-128

STPPER MOTOR ALGORITHM

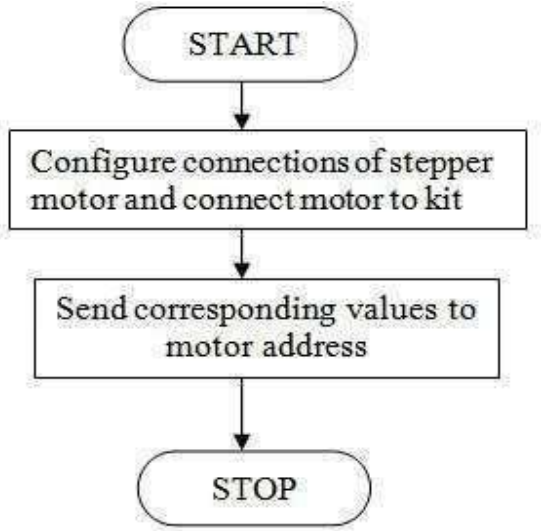
STEP1: Configure the hardware connections of STEPPER Motor.

STEP2: Connect the STEPPER Motor to J4 connector of 8051 SDK kit.

STEP3: To run Stepper Motor in FARWORD Direction send 0x01, 0x02, 0x04, 0x08 sequence of data one at a time to the STEPPER MOTOR ADDRESS

STEP4: To run Stepper Motor in REVERSE Direction send 0x08, 0x04, 0x02, 0x01 Sequence of data one at a time to the STEPPER MOTOR ADRRESS

STEP5: End



PROGRAM FOR STEPPER MOTOR

```
#include<REGX51.H>

void delay(unsigned int d);

int main(void)
{
	while(1)
	{
		P2=0x01;
		delay(1000);
		P2=0x02;
		delay(1000);
		P2=0x04;
		delay(1000);
		P2=0x08;
		delay(1000);
	}
}

void delay(unsigned int d)
{
	unsigned int i,j;
	for(i=0;i<d;i++)
	for(j=0;j<101;j++);
}
```

Program Validation

Input :

1. Stepper(10,1) , Here count=10 and direction=1.
2. Stepper(10,0) , Here count=10 and direction=0.

Output :

1. When count=10 and direction=1 which means the stepper motor rotates for 10 counts in clockwise direction with a delay after each count.
2. Here count=10 and direction=0 which means stepper motor rotates for 10 counts in anticlockwise direction with a delay after each count.

Conclusion:

The program to demonstrate Stepper Motor using 8051 Microcontroller development kit executed successfully.

Program 6
LCD

Program Definition

To write a program to demonstrate LCD using 8051 Microcontroller development kit.

General Description:

The Liquid Crystal Display (LCD) is a low power device (microwatts). Now a days in most applications LCDs are using rather using of LED displays because of its specifications like low power consumption, ability to display numbers and special characters which are difficult to display with other displaying circuits and easy to program. An LCD requires an external or internal light source. Temperature range of LCD is 0ºC to 60ºC and lifetime is an area of concern, because LCDs can chemically degrade these are manufactured with liquid crystal material (normally organic for LCDs) that will flow like a liquid but whose molecular structure has some properties normally associated with solids.

LCDs are classified as

- Dynamic-scattering LCDs and
- Field-effect LCDs

Field-effect LCDs are normally used in such applications where source of energy is a prime factor (e.g., watches, portable instrumentation etc.).They absorb considerably less power than the light-scattering type. However, the cost for field-effect units is typically higher, and their height is limited to 2 inches. On the other hand, light-scattering units are available up to 8 inches in height. Field-effect LCD is used in the project for displaying the appropriate information.

RS (Command / Data):

This bit is to specify weather received byte is command or data. So that LCD can recognize the operation to be performed based on the bit status.

RS = 0 => Command
RS = 1 => Data

RW (Read / Write):

RW bit is to specify whether controller wants READ from LCD or WRITE to LCD. The READ operation here is just ACK bit to know whether LCD is free or not.

RW = 0 => Write
RW = 1 => Read

EN (Enable LCD):

EN bit is to ENABLE or DISABLE the LCD. When ever controller wants to write some thing into LCD or READ acknowledgment from LCD it needs to enable the LCD.

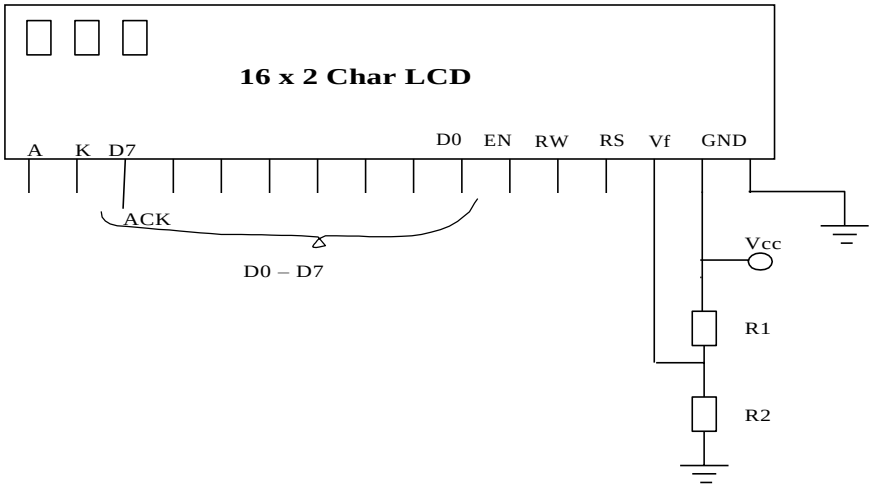
EN = 0 => High Impedance
EN = 1 => Low Impedance

ACK (LCD Ready):

ACK bit is to acknowledge the MCU that LCD is free so that it can send new command or data to be stored in its internal Ram locations

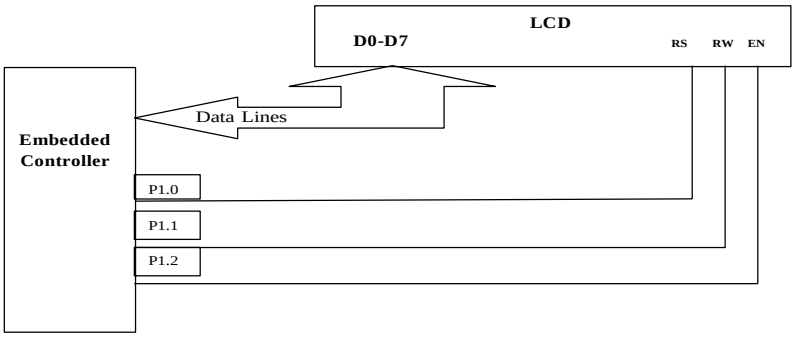
ACK = 1 => Not ACK
ACK = 0 => ACK

LCD diagram:



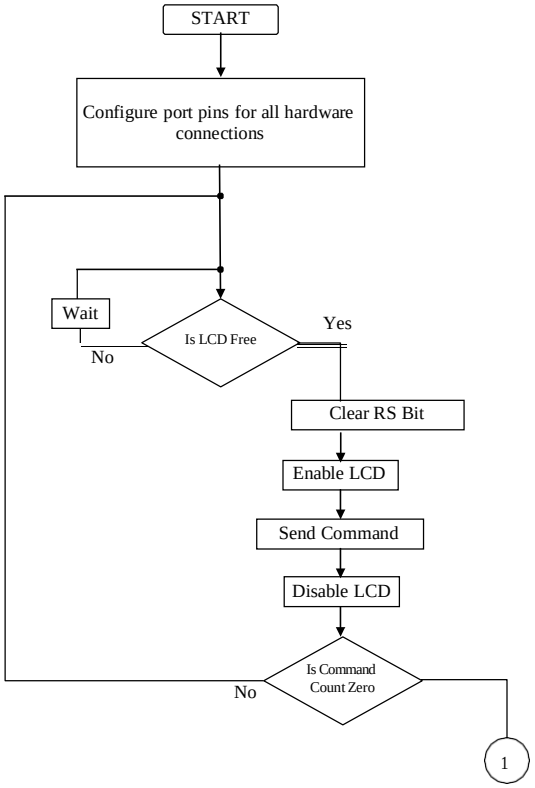
Block Diagram

Hardware connections:



CONTROLER PINS	LCD PINS	PIN NAME WITH FEATURE
(P1.0)	4	RS (Control Pin)
(P1.1)	5	RW (Control pin)
(P1.2)	6	EN (Control pin)
Port 0	7 to 14	Data Port
40	15 & 2	Vcc
20	16 & 1	Gnd

FLOWCHART:



Program Description

In this program, we try to display characters in LCD display. 16×2 characters can be displayed. Here we need to initialize the LCD first using **lcdinit(void).** When LCD is initialized ,we store all commands in an array **ledtable[]**. Now put commands on LCD using **put_com(ledtable[i])** then **lcd_check()** is called i.e., it checks LCD value clears all the contents of previous ones using ***lcd_display=0x00.** Then the characters to be displayed are provided using the function call **put_char('char',address).**

Algorithm

1. Initialize Set of Commands.
2. Initialize LCD with proper set of Commands.
3. Write each Command to LCD Command Write Address.
4. Clear LCD for any prev data.
5. Write Data to LCD Data Write Address.

PROGRAM TO DISPLAY ROLL NO & NAME USING LCD:

```
#include<REGx51.H>
#define LCD P0
#defineRS P3_4
#define EN P3_5
void lcdInit(void);
void putComL(unsigned char);
void putCharL(unsigned char);
void putStrL(unsigned char*,unsigned char);
void delay(unsigned int d);
int main(void)
{
        lcdInit();
        delay(1000);
        putStrL("ABDUL HADI",0x01);
        putStrL("032",0xc0);
        while(1);
}
void lcdInit(void)
{
        putComL(0x38);
        putComL(0x0c);
        putComL(0x06);
        putComL(0x01);
        putComL(0x80);
}
void putComL(unsigned char cmd)
{
        RS=0;
        LCD=cmd;
        EN=1;
        delay(100);
        EN=0;
}
void putCharL(unsigned char dat)
{
        RS=1;
        LCD=dat;
        EN=1;
```

```
        delay(100);
        EN=0;
}
void putStrL(unsigned char *str,unsigned char cmd)
{
        unsigned char i=0;
        putComL(cmd);
        while(*str)
                {
                        i++;
                        if(i==17)
                        putComL(0xc0);
                        putCharL(*str++);
                }}

 void delay(unsigned int d)
 {
        unsigned int i,j;
        for(i=0;i<d;i++)
        for(j=0;j<101;j++);
```

Program Validation

Input: PRATHYUSHA OK

Output:

The string displayed on LCD .

Conclusion:

The program to demonstrate LCD using 8051 microcontroller development kit is executed successful.

PROGRAM 7
KEYPAD

Program Definition

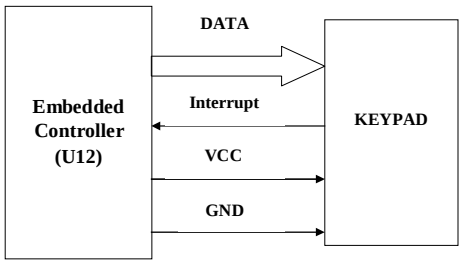
To write a program to demonstrate Keypad using 8051 Microcontroller development kit.

Keypad connector

In this product we have to design the 8 keys keypad directly connecting the 8 keys into 8 pins of Micro Controller. In this board we have to adding the extra feature like Matrix Keypad. In this 8 pins of AT89C51 are connected to the Keypad Connector. Matrix keypads such 4 by 4 can be connected directly to the connector. 5 Volt and Ground power lines are also available on the connector.

These two types of features are only working with any one external interrupt because of every key pressing its generating the interrupt.

Block diagram:



Hardware Connections:

CONTROLER PINS	KEYPAD	PIN NAME	FEATURE
P0.7 TO P0.2 & P0.1,P0.0	SW1 TO SW6 & 8,9	DATA	DATA
P3.3(INT1)	interrupt	CLK	Interrupt
20		GND	
40		VCC	

Program Description

Keypad is a widely used input device with lots of application in our everyday life. In Toll Gate Indicator Signal Lights the above concept of pressing the key and glowing of LED is used for effective traffic divert.

In this program, we demonstrate keypad wherein when a key is pressed, corresponding LED glows. When a key is pressed, some interrupts is given, which is connected to a port in Microcontroller and so LED glows.

Val=getchar() , val stores the character which is pressed using the function getchar() IE-Interrupt enable, IP-Interrupt Priority, ITI-Interrupt Timer are initialized and **Led(val)** led function is called.

Algorithm

KEYBOARD ALGORITHAM

STEP1: Verify the PS2 connector connections which pins are connected to Microcontroller as data (P1.5) and clock (INT0) pins.

STEP2**:** Initialize the LCD by passing a set of COMMANDS

STEP3: Initialize the Keyboard by loading proper values in IE, IP registers and set the ITx (Interrupt Type) bit of corresponding Interrupt

STEP4**:** Microcontroller waits until press a key. When a key is pressed Interrupts will occur and key flag is set.

STEP5**:** Pressed key will generate a scan code and interrupt (key flag is set), this scan code is compared with the Table what we are mentioned.

COMPARISON WITH CAPS LOCK KEY

STEP6: If the first scan code matches to the CAPS LOCK scan code then cap Flag will complement

STEP7: If the CAPS LOCK is already ON it will OFF (or) If the CAPS LOCK is OFF it will ON

STEP8: Next pressed key scan code will compare with the CAPS lock Table

STEP9**:** Display the corresponding key in LCD or SERIAL

COMPARISON WITH SHIFT KEY

STEP10: If the **first scan code** matches to the LSHIFT (left shift) or RSHIFT (right shift) Scan code then set the shift Flag

STEP11: Now compare the second scan code if the **second scan code** is not equal to **8051-SDK**

Release scans code (0xF0) display the corresponding key value from the SHIFT Table

STEP12: if the **second scan code** is **equal** to Release scan code (0xF0) then break the Comparison and wait for press a key.

COMPARISON WITH NORMAL KEY

STEP13: If the **first scan code** not matches with the CAPS LOCK, LSHIFT (left shift) And RSHIFT (right shift) scan codes then compare the first scan code with the Unthrift (or) Normal Table values

STEP14: Display the corresponding key in LCD or SERIAL.

STEP15: End

Program:

```
#include<REGX51.H>
#include "lcd.h"
#include "delay.h"
unsigned char keyScan(void);
 #define row1 P1_0
 #define row2 P1_1
 #define row3 P1_2
 #define row4 P1_3
 #define  col1  P1_4
 #define  col2  P1_5
 #define  col3  P1_6
 #define col4 P1_7

 int main (void)
  {
        unsigned char key;
        lcdInit();
        putStrL("KEY TEST",0X01);
        putComL(0XC0);

        while(1)
        {
              key=keyScan();
              putCharL(key);
              delay(1000);
        }
  }
```

```
unsigned char keyScan(void)
{
        row1=row2=row3=row4=1;
        col1=col2=col3=col4=0;
        while(row1&row2&row3&row4);
        if(!row1)
        {
                col1=1;
                if(row1)
                {       col1=0;
                while(!row1);
                return('1');
        }
         col1=0;
         col2=1;
         if(row1)
         {
         col2=0;
         while(!row1);
         return('2');
         }
         col2=0;
         col3=1;
         if(row1)
         {
         col3=0;
         while(!row1);
         return('3');
         }
         col3=0;
         col4=1;
         if(row1)
         {
         col4=0;
         while(!row1);
         return('^');
         }
         col4=0;
         }

         else if(!row2)
         {
         col1=1;
         if(row2){
         col1=0;
         while(!row2);
```

```
 return('4');
 }
 col1=0;
 col2=1;
 if(row2){
 col2=0;
 while(!row2);
 return('5');
 }
 col2=0;
 col3=1;
 if(row2){
 col3=0;
 while(!row2);
 return('6');
 }
 col3=0;
 col4=1;
 if(row2)
 {
 col4=0;while(!row2);return('V');}
 col4=0;
 }

else if(!row3)
 {
 col1=1;
 if(row3)
 {
 col1=0;
 while(!row3);
 return('7');
 }
 col1=0;
 col2=1;
 if(row3)
 {
 col2=0;
 while(!row3);
 return('8');
 }
 col2=0;
 col3=1;
 if(row3)
 {
 col3=0;
```

```
  while(!row3);
  return('9');
  }
  col3=0;
  col4=1;
  if(row3)
  {
  col4=0;
  while(!row3);
  return('M');
  }
  col4=0;
  }
  else if(!row4)
  {
  col1=1;
  if(row4)
  {
  col1=0;
  while(!row4);
  return('*');
  }
  col1=0;
  col2=1;
  if(row4)
  {
  col2=0;
  while(!row4);
  return('0');
  }
  col2=0;
  col3=1;
  if(row4)
  {
  col3=0;
  while(!row4);
  return('#');
  }
  col3=0;
 col4=0;
 if(row4)
  {
  col4=0;
  while(!row4);
  return('E');
  }
```

```
col4=0;
}
return 0;
}
```

Program Validation

Input :

key 28 is pressed , val=28 is passed to led()

Output:

LED 2 glows. Similarly for any key pressed its corresponding LED glows .

Conclusion :

Program to demonstrate Keypad using 8051 Microcontroller development kit was successfully executed.

Program 8
ELEVATOR CONTROLLER

Program Definition

To Write a program to demonstrate Elevator Controller using 8051 Microcontroller development kit.

Program Description

First we initialize variable loc=0X01, Then put „loc" value in variable prev. The key which is pressed is put into „loc" using ***getchar8().*** Then we check whether „loc" is greater or less than or equal to „prev".

- If (loc<prev) Elevator moves downwards .
- When (loc==prev) → the LED stops there at that position.
- If (loc>prev) Elevator moves upwards.

Algorithm

1. Initialize Elevator to Ground Floor (LED 1 Glows)
2. While true
3. Press Keypad switch to select particular floor
4. Rotate stepper motor clockwise or anti clockwise depending upon the key press
5. Glow the LED of particular floors as stepper motor rotates
6. Repeat steps 3, 4, and

ELEVATOR:

```
#include<REGX51.h>
void delay(unsigned int d);
code unsigned char seg7[10]={0XC0,0XF9,0XA4,0XB0,0X99,0X92,0X82,0XF8,0X80,0X90};
code unsigned char motoru[8]={0X01,0X03,0X02,0X06,0X04,0X0C,0X08,0X09};
code unsigned char motord[8]={0X09,0X08,0X0C,0X04,0X06,0X02,0X03,0X01};

int main (void)
{
unsigned char loc,pre=0X01,seg=0,i,j;
loc=pre;
P3_5=1;
P2=pre;
P1=0XFF;
P0=seg7[seg];
```

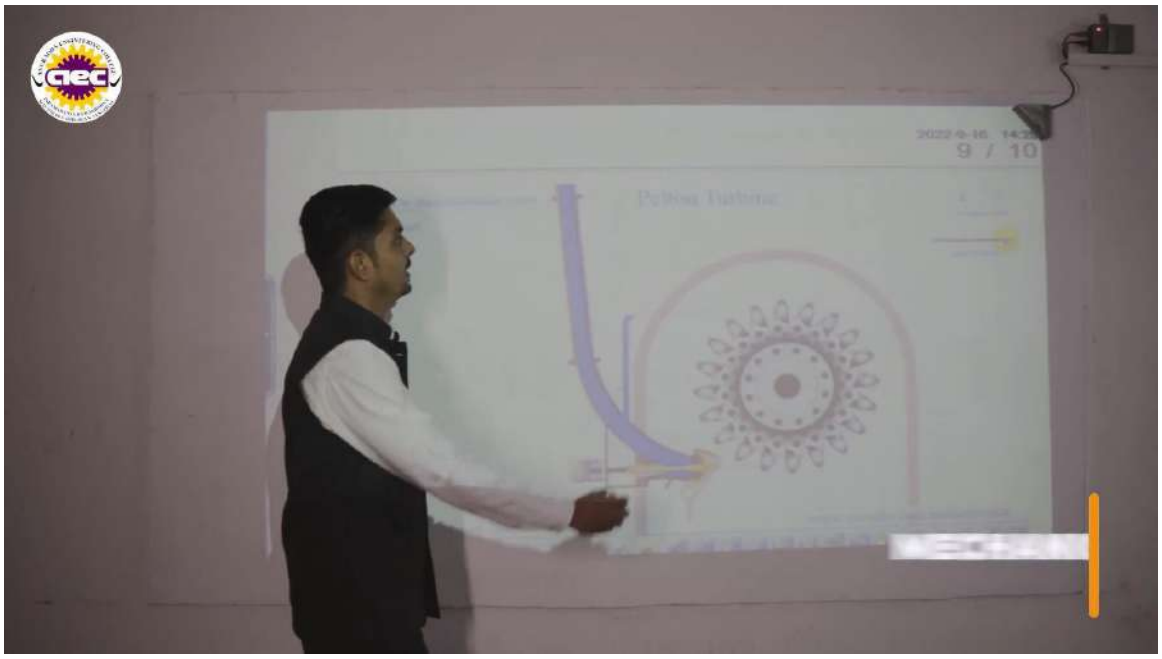
```
while(1)
{
P1=0XFF;
while(P1==0XFF);
loc=~P1;
if(loc<pre)
{
while(loc!=pre)
{
pre=pre>>1;
seg--;
for(j=0;j<4;j++)
for(i=0;i<8;i++)
{
P2=motoru[i];
delay(50);
}
P0=seg7[seg];
}
}
else if(loc>pre)
{
while(loc!=pre)
{
  pre=pre<<1;
seg++;
for(j=0;j<4;j++)
for(i=0;i<8;i++)
{
P2=motord[i];
delay(50);
}
P0=seg7[seg];
}
}
}
}
void delay(unsigned int d)
{
unsigned int i,j;
 for(i=0;i<=d;i++)
 for(j=0;j<101;j++);
 }
```

ELEVATOR OUTPUT:-

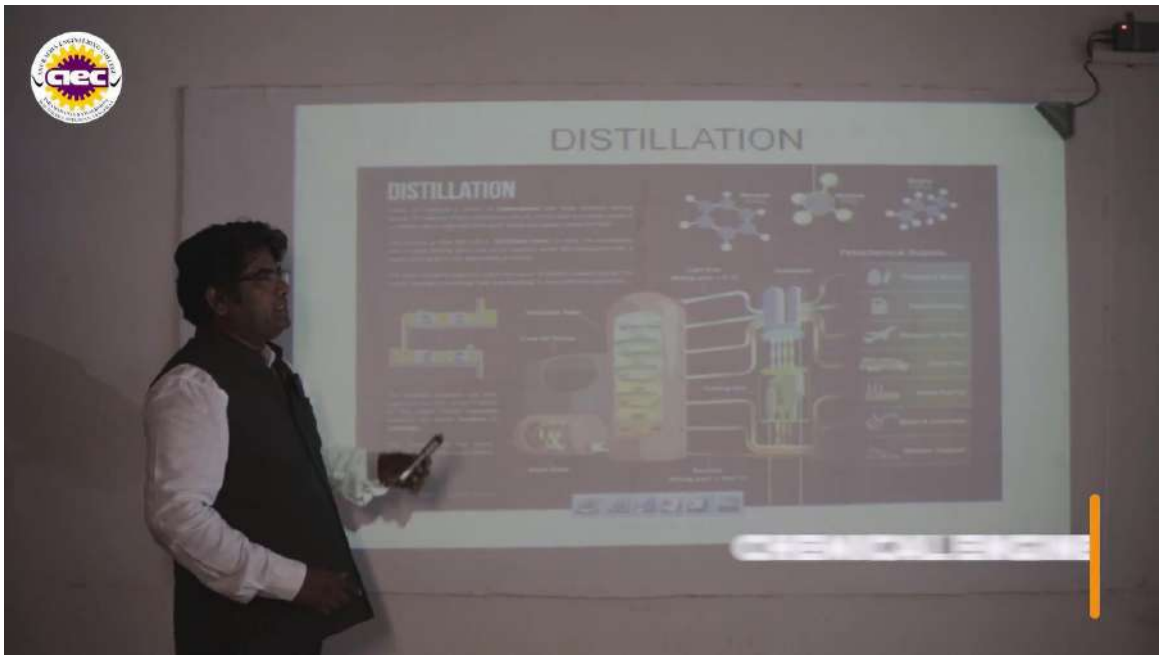
Conclusion:

The C program to demonstrate Elevator controller was executed successfully using 8051 Microcontroller development

- **11. Photos Showing Use of ICT**

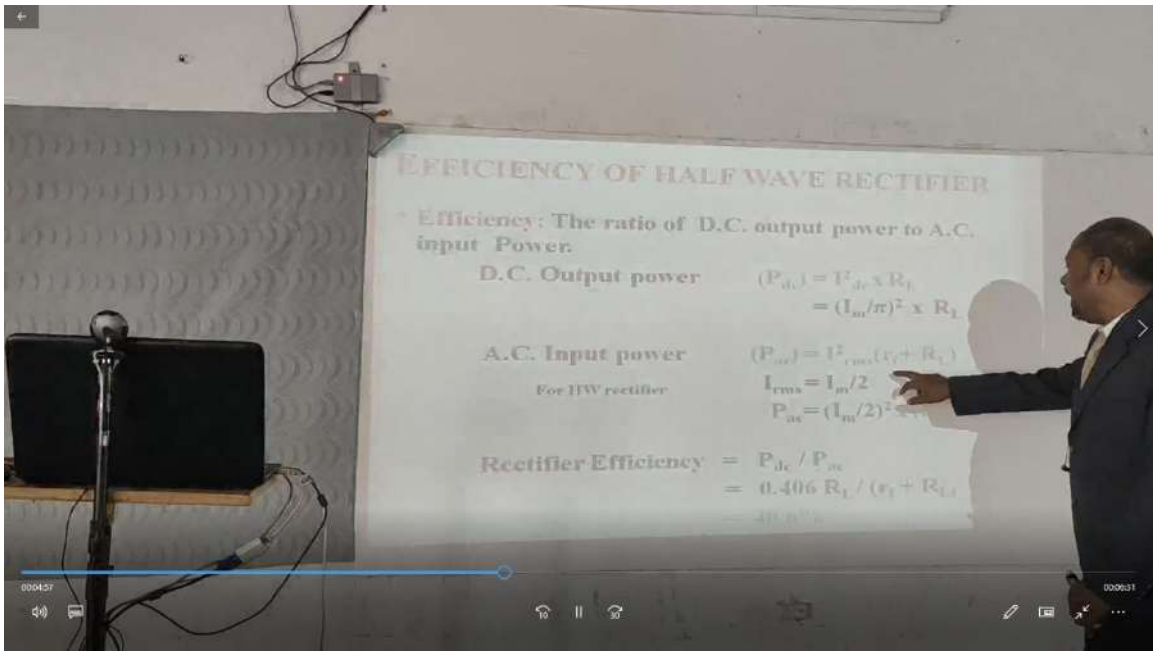


Class Room

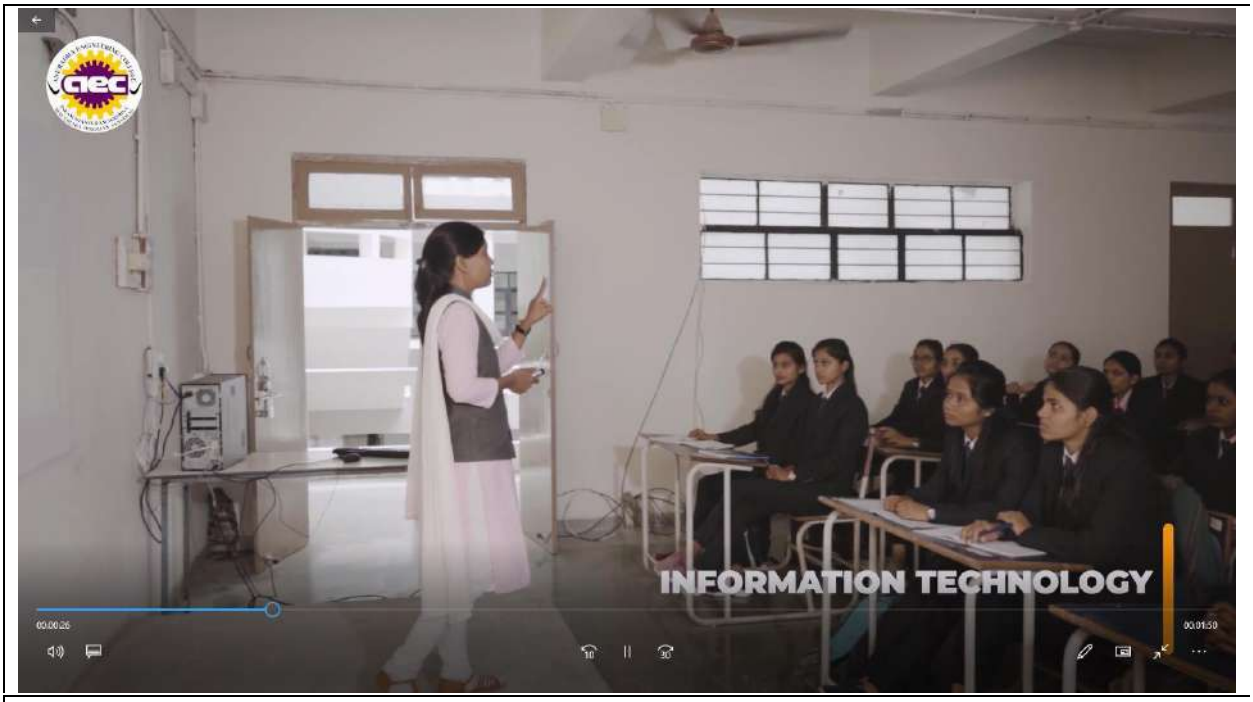


Class Room

Class Room

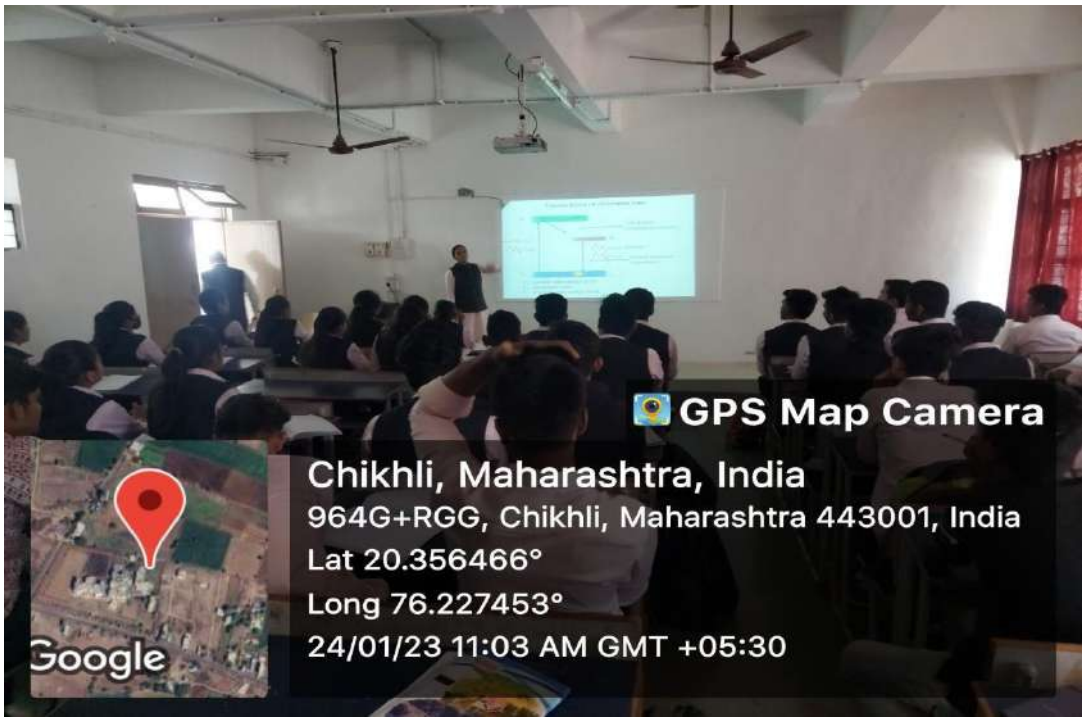


Class Room



Class Room

Class Room



Class Room

Class Room

Class Room

Class Room

12 Academic Audit Report submitted by Institutional IQAC to CDC

Paramhansa Ramkrishna Mauniboba Shikshan Sanstha's

ANURADHA ENGINEERING COLLEGE

Internal Quality Assurance Cell

To,
The Chairman,
College Development Committee,
Anuradha Engineering College, Chikhli

Date: 23/06/2023

Subject: Submission of Internal Academic Audit Report for the Academic Year 2022-23

Respected sir,

I am writing to formally submit the Internal Academic Audit Report for the academic year 2022-23 of Anuradha Engineering College, Chikhli. The report has been meticulously prepared by the Internal Quality Assurance Cell (IQAC), and I am pleased to present it to the College Development Committee for your perusal and consideration.

This report encapsulates the outcomes of our academic audit, covering various aspects of our institution's academic performance, quality of education, and adherence to the standards set by regulatory bodies. The undersigned and the IQAC team have worked diligently to collect and analyze data, assess the effectiveness of our academic processes, and identify areas of improvement. The audit process included a comprehensive review of our curriculum, faculty performance, assessment methods, infrastructure, student feedback, and compliance with statutory regulations.

I kindly request the College Development Committee to allocate time for a thorough review of this report during your upcoming meetings. The IQAC team will be available to provide any clarifications or additional information as required. We are committed to working in collaboration with the committee to implement the recommended improvements and continually raise the academic excellence of our college.

Please find attached the Internal Academic Audit Report for the academic year 2022-23. Your feedback and insights are highly valued and will be integral to our efforts to maintain and improve the quality of education provided by the institute.

Thank you for your attention to this matter, and I look forward to your valuable input and guidance in this regard.

Yours sincerely,

Dr. P. S. Gawande

IQAC Coordinator

IQAC Coordinator
Anuradha Engineering College
Chikhli, Dist. Buldhana.

Paramhansa Ramkrishna Maunibaba Shikshan Sanstha's

ANURADHA ENGINEERING COLLEGE

Internal Academic Audit Report 2022-23

Academic audit is a vital aspect of maintaining and enhancing the quality of education at Anuradha Engineering College carried out both internal and external assessments at the departmental level. This report summarizes the findings and observations of the academic audit, which includes internal evaluations and external evaluations carried out by faculty from other institutions.

Students Performance & Result:

The performance of our students is continuously evaluated through a variety of assessment methods, including internal evaluations, unit tests, viva voce, assignments, seminars, and presentations. The IQAC (Internal Quality Assurance Cell) has observed that the academic performance of our students is exemplary. This conclusion is further supported by positive feedback from students regarding the faculty's teaching quality. The IQAC is highly satisfied with the students' academic performance and their active participation in co-curricular activities.

Student-Faculty Ratio & Mentor Mentee Ratio:

The Student-Faculty Ratio and Mentor Mentee Ratio are key indicators of the institution's commitment to providing personalized attention and guidance to students. The IQAC has found these ratios to be satisfactory, reflecting our dedication to maintaining a favorable learning environment.

Feedback Form Analysis:

The D-IQAC (Departmental Internal Quality Assurance Cell) has collected feedback from various stakeholders, including students, faculty, parents, employers, and alumni. An action report has been prepared based on this feedback to address any concerns and continuously improve the academic experience.

University & Examination Cell:

The IQAC closely monitors the University & Examination Cell to ensure the timely and efficient conduction of internal examinations and other evaluation components. The IQAC has found no discrepancies in the execution and conduction of these evaluation processes. We are satisfied with the Examination Cell's performance.

Information Technology (IT):

The IQAC has evaluated the IT facilities, including internet access, computer systems, and printers, available on the campus. We are highly appreciative of the IT resources, which meet the standards of excellence in connectivity, availability, and accessibility.

Hostel:

The IQAC assessed the hostel facilities, including amenities like drinking water provided through the institute's RO plant, availability of hot water, room conditions, and AC facilities. We are pleased to report that these facilities are on par with the best, ensuring a comfortable and conducive environment for our students.

Canteen:

The IQAC conducted a thorough inspection of the canteen, focusing on cleanliness, hygiene, food quality, and the condition of cutlery. We are pleased to note that all aspects were found to be in precise order, reflecting the staff's commitment to maintaining high standards of cleanliness and hygiene.

Transport:

The transport facility, including the condition of buses, compliance with safety measures, and pick-up and drop-off services for students, was audited by the IQAC. We are satisfied with the condition and safety standards of the transport services, which ensure the well-being of our students.

Financial Audit:

The institute conducts both internal and external financial audits, with both audits being carried out by CA Bhagwan Nagwani and Company. Internal audits are conducted quarterly, while external audits are performed annually, ensuring financial transparency and accountability.

Here are aspects for improvement in the academic context:

- Increase the number of programs attended in other institutes and those organized in-house by faculty and students.
- Arrange more industrial visits for the students to enhance their practical exposure.
- Boost the number of research publications by both faculty and students to contribute to academic advancement.
- Initiate student chapters in all departments to promote academic engagement and collaboration.
- Enhance the count of professional body memberships among students and faculty.
- Implement additional skill development programs for students to equip them with relevant competencies.

IQAC Co-ordinator
Anuradha Engineering College
Chikhli, Dist. Buldhana.

Arun Narayan Nanhai

Digitally signed by Arun Narayan Nanhai
DN: c=IN, o=Personal, title=9481, pseudonym=6FtRn86oloSk9GfxzyGyj4qDFXp5z0BZ, 2.5.4.20=aebd8eb98f199d4a040d7db461ef0a25271c0f59aa1ae78ce570fb2d6f81c07e, postalCode=443201, st=Maharashtra, serialNumber=4d9109a773dee89ab04bcb9bd1f389f834b3072351afd1237358ec53fda32b09, cn=Arun Narayan Nanhai
Date: 2024.01.21 16:41:12 +05'30'

Principal, Anuradha Engineering College, Chikhli